



US009048327B2

(12) **United States Patent**
Tanaka et al.

(10) **Patent No.:** **US 9,048,327 B2**
(45) **Date of Patent:** **Jun. 2, 2015**

(54) **MICROCRYSTALLINE SEMICONDUCTOR FILM, METHOD FOR MANUFACTURING THE SAME, AND METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE**

USPC 438/164, 158, 479, 482; 257/E21.091,
257/E21.618, E21.412
See application file for complete search history.

(75) Inventors: **Tetsuhiro Tanaka**, Kanagawa (JP);
Takashi Ienaga, Kanagawa (JP); **Ryu Komatsu**, Kanagawa (JP); **Erika Kato**, Kanagawa (JP); **Ryota Tajima**, Kanagawa (JP); **Yasuhiro Jinbo**, Kanagawa (JP)

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,409,134 A 10/1983 Yamazaki
5,453,858 A 9/1995 Yamazaki

(Continued)

FOREIGN PATENT DOCUMENTS

EP 0 535 979 A2 4/1993
JP 04-242724 8/1992

(Continued)

OTHER PUBLICATIONS

Arai et al., "41.2: Micro Silicon Technology for Active Matrix OLED Display", SID Digest 07 : SID International Symposium Digest of Technical Papers, 2007, vol. 38, pp. 1370-1373.

(Continued)

(73) Assignee: **Semiconductor Energy Laboratory Co., Ltd.**, Kanagawa-ken (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 406 days.

(21) Appl. No.: **13/355,340**

(22) Filed: **Jan. 20, 2012**

(65) **Prior Publication Data**

US 2012/0187408 A1 Jul. 26, 2012

(30) **Foreign Application Priority Data**

Jan. 25, 2011 (JP) 2011-012496

(51) **Int. Cl.**

H01L 21/00 (2006.01)
H01L 29/786 (2006.01)
H01L 21/02 (2006.01)
H01L 29/04 (2006.01)
H01L 29/66 (2006.01)

(52) **U.S. Cl.**

CPC **H01L 29/78696** (2013.01); **H01L 21/02598** (2013.01); **H01L 29/78654** (2013.01);
(Continued)

(58) **Field of Classification Search**

CPC H01L 21/02532; H01L 21/02592;
H01L 21/0262; H01L 29/41733; H01L 29/78663; H01L 21/091; H01L 21/02598;
H01L 29/78654

Primary Examiner — William F Kraig

Assistant Examiner — Joseph C Nicely

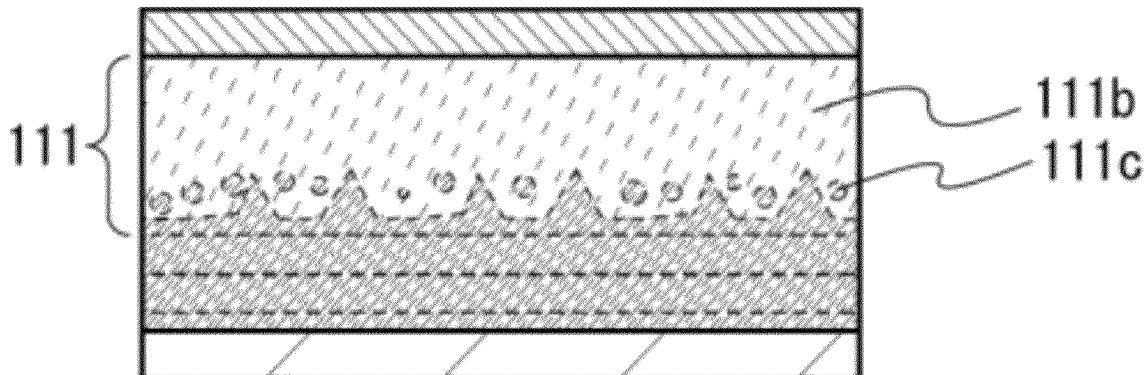
(74) *Attorney, Agent, or Firm* — Nixon Peabody LLP;
Jeffrey L. Costellia

(57)

ABSTRACT

An embodiment of the present invention is a microcrystalline semiconductor film having a thickness of more than or equal to 70 nm and less than or equal to 100 nm and including a crystal grain partly projecting from a surface of the microcrystalline semiconductor film. The crystal grain has an orientation plane and includes a crystallite having a size of 13 nm or more. Further, the film density of the microcrystalline semiconductor film is higher than or equal to 2.25 g/cm³ and lower than or equal to 2.35 g/cm³, preferably higher than or equal to 2.30 g/cm³ and lower than or equal to 2.33 g/cm³.

21 Claims, 17 Drawing Sheets



(52) U.S. Cl.

CPC *H01L21/02422* (2013.01); *H01L 21/0245*
(2013.01); *H01L 21/02502* (2013.01); *H01L*
21/02513 (2013.01); *H01L 21/02532* (2013.01);
H01L 21/02595 (2013.01); *H01L 21/0262*
(2013.01); *H01L 29/04* (2013.01); *H01L*
29/66765 (2013.01); *H01L 29/78648* (2013.01);
H01L 29/78678 (2013.01)

2012/0012851 A1 * 1/2012 Yamazaki et al. 257/59
2012/0100675 A1 * 4/2012 Komatsu et al. 438/158
2012/0108055 A1 * 5/2012 Yoshimura et al. 438/637
2012/0115285 A1 * 5/2012 Komatsu et al. 438/157
2013/0056742 A1 * 3/2013 Tezuka et al. 257/66
2013/0334525 A1 * 12/2013 Miyairi et al. 257/43
2014/0097499 A1 * 4/2014 Parekh et al. 257/368
2014/0178861 A1 * 6/2014 Duer 435/5
2014/0180251 A1 * 6/2014 Ferrari et al. 604/513

(56)

References Cited

U.S. PATENT DOCUMENTS

5,514,879 A 5/1996 Yamazaki
5,571,578 A 11/1996 Kaji et al.
5,582,880 A 12/1996 Mochizuki et al.
5,591,987 A 1/1997 Yamazaki et al.
5,614,732 A 3/1997 Yamazaki
5,648,293 A 7/1997 Hayama et al.
5,677,236 A 10/1997 Saitoh et al.
5,701,167 A 12/1997 Yamazaki
5,849,601 A 12/1998 Yamazaki
5,859,445 A 1/1999 Yamazaki
6,011,277 A 1/2000 Yamazaki
6,023,075 A 2/2000 Yamazaki
6,153,893 A 11/2000 Inoue et al.
6,252,249 B1 6/2001 Yamazaki
6,265,288 B1 7/2001 Okamoto et al.
6,271,055 B1 8/2001 Yajima et al.
6,281,520 B1 8/2001 Yamazaki
6,306,213 B1 10/2001 Yamazaki
6,344,420 B1 2/2002 Miyajima et al.
6,468,839 B2 10/2002 Inoue et al.
6,737,676 B2 5/2004 Yamazaki
6,855,621 B2 2/2005 Kondo et al.
7,067,844 B2 6/2006 Yamazaki
7,098,479 B1 8/2006 Yamazaki
7,115,902 B1 10/2006 Yamazaki
7,551,655 B2 6/2009 Tanaka et al.
7,576,360 B2 8/2009 Yamazaki
7,833,845 B2 11/2010 Yamazaki et al.
8,383,434 B2 * 2/2013 Isa 438/30
8,426,295 B2 * 4/2013 Komatsu et al. 438/485
8,450,158 B2 * 5/2013 Komatsu et al. 438/151
2009/0002591 A1 1/2009 Yamazaki et al.
2009/0033818 A1 2/2009 Nakajima et al.
2009/0047759 A1 * 2/2009 Yamazaki et al. 438/158
2009/0047774 A1 * 2/2009 Yamazaki 438/479
2009/0057683 A1 3/2009 Nakajima et al.
2009/0061574 A1 3/2009 Nakajima et al.
2009/0072237 A1 * 3/2009 Yamazaki et al. 257/72
2009/0133753 A1 * 5/2009 Sasaki et al. 136/261
2009/0140250 A1 * 6/2009 Yamazaki et al. 257/57
2009/0189256 A1 * 7/2009 Yoshimura et al. 257/621
2009/0219653 A1 * 9/2009 Aoki et al. 360/294.4
2009/0276078 A1 * 11/2009 Sugamoto et al. 700/121
2009/0321737 A1 * 12/2009 Isa et al. 257/57
2010/0124804 A1 * 5/2010 Takahashi et al. 438/158
2010/0216285 A1 * 8/2010 Yokoi et al. 438/158
2010/0266898 A1 * 10/2010 Yamamoto et al. 429/220
2011/0020989 A1 * 1/2011 Tajima et al. 438/158
2011/0039402 A1 * 2/2011 Yamazaki et al. 438/488
2011/0056435 A1 * 3/2011 Yamazaki 118/723 R
2011/0059562 A1 3/2011 Yamazaki et al.
2011/0101354 A1 * 5/2011 Saito et al. 257/59
2011/0147745 A1 * 6/2011 Sasagawa et al. 257/57
2011/0147755 A1 * 6/2011 Miyairi et al. 257/60
2011/0177396 A1 * 7/2011 Moriwaka et al. 429/304
2011/0204364 A1 * 8/2011 Isa 257/57
2011/0217811 A1 * 9/2011 Tanaka et al. 438/97
2011/0272700 A1 * 11/2011 Yamaguchi et al. 257/66
2011/0278582 A1 * 11/2011 Tezuka et al. 257/66
2011/0306158 A1 * 12/2011 Tan 438/51
2011/0318888 A1 * 12/2011 Komatsu et al. 438/157
2011/0318896 A1 * 12/2011 Ohnuma 438/300
2012/0001178 A1 * 1/2012 Miyairi et al. 257/53
2012/0007210 A1 * 1/2012 Shih 257/506

FOREIGN PATENT DOCUMENTS

JP 05-129608 5/1993
JP 05-275346 10/1993
JP 06-077483 3/1994
JP 07-045833 2/1995
JP 07-131030 5/1995
JP 07-162003 6/1995
JP 07-211708 8/1995
JP 09-232235 9/1997
JP 2000-174310 6/2000
JP 2000-269201 9/2000
JP 2000-277439 10/2000
JP 2001-053283 2/2001
JP 3201492 8/2001
JP 2002-206168 7/2002
JP 2002-246605 8/2002
JP 2002-280309 9/2002
JP 2003-037278 2/2003
JP 2004-200345 7/2004
JP 2005-049832 2/2005
JP 2005-167264 6/2005
JP 2005-191546 7/2005
JP 2006-237490 9/2006
JP 2009-044134 2/2009
JP 2009-076753 4/2009
JP 2009-088501 4/2009

OTHER PUBLICATIONS

Lcc et al., "How to Achieve High Mobility Thin Film Transistors by Direct Deposition of Silicon Using 13.56 MHz RF PECVD?", IEDM 06: Technical Digest of International Electron Devices Meeting, Dec. 11, 2006, pp. 295-298.
Lee et al., "Directly Deposited Nanocrystalline Silicon Thin-Film Transistors with Ultra High Mobilities", Applied Physics Letters, Dec. 18, 2006, vol. 89, No. 25, pp. 252101-1-252101-3.
Lee et al., "High-Mobility Nanocrystalline Silicon Thin-Film Transistors Fabricated by Plasma-Enhanced Chemical Vapor Deposition", Applied Physics Letters, May 24, 2005, vol. 86, pp. 222106-1-222106-3.
Lcc et al., "High Mobility N-Channel and P-Channel Nanocrystalline Silicon Thin-Film Transistors", IEDM 05: Technical Digest of International Electron Devices Meeting, 2005, pp. 937-940.
Esmaili-Rad et al., "High Stability, Low Leakage Nanocrystalline Silicon Bottom Gate Thin Film Transistors for AMOLED Displays", IEDM 06: Technical Digest of International Electron Devices Meeting, 2006, pp. 303-306.
Lee et al., "Leakage Current Mechanisms in Top-Gate Nanocrystalline Silicon Thin Film Transistors", Applied Physics Letter, Feb. 28, 2008, vol. 92, pp. 083509-1-083509-3.
Esmaili-Rad et al., "Absence of Defect State Creation in Nanocrystalline Silicon Thin Film Transistors Deduced from Constant Current Stress Measurements", Applied Physics Letters, Sep. 12, 2007, vol. 91, No. 11, pp. 113511-1-113511-3.
Lee et al., "Stability of nc-Si:H TFTs with Silicon Nitride Gate Dielectric", IEEE Transaction on Electron Devices, 2007, vol. 54, No. 1, pp. 45-51.
Sazonov et al., "Low-Temperature Materials and Thin Film Transistors for Flexible Electronics", Proceedings of the IEEE, Aug. 1, 2005, vol. 93, No. 8, pp. 1420-1428.
Lee et al., "Postdeposition Thermal Annealing and material Stability of 75° C. Hydrogenated Nanocrystalline Silicon Plasma-Enhanced Chemical Vapor Deposition Films", Journal of Applied Physics, Aug. 4, 2005, vol. 98, No. 3, pp. 034305-1-034305-7.

* cited by examiner

FIG. 1A

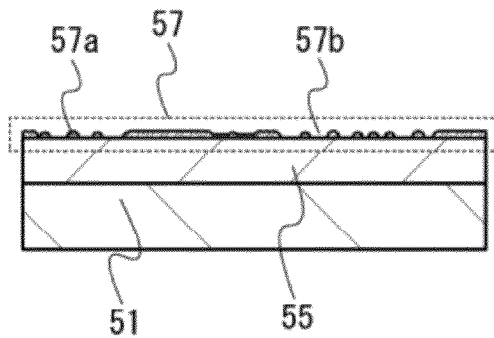


FIG. 1D

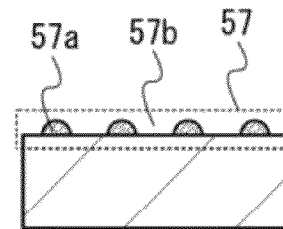


FIG. 1E

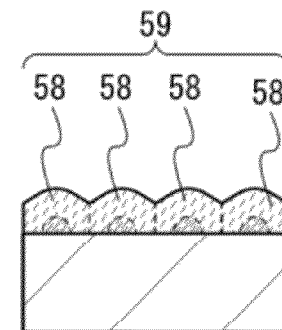


FIG. 1B

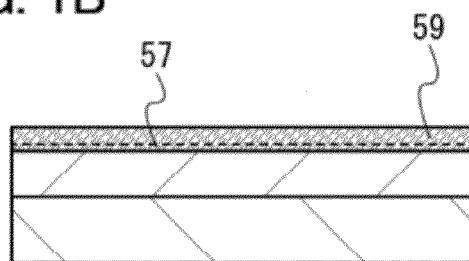


FIG. 1C

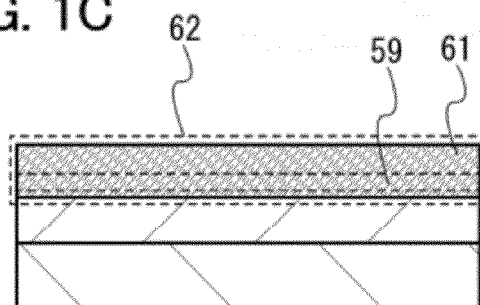


FIG. 1F

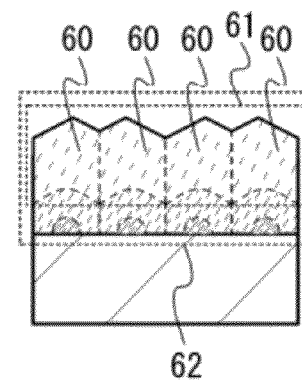


FIG. 2

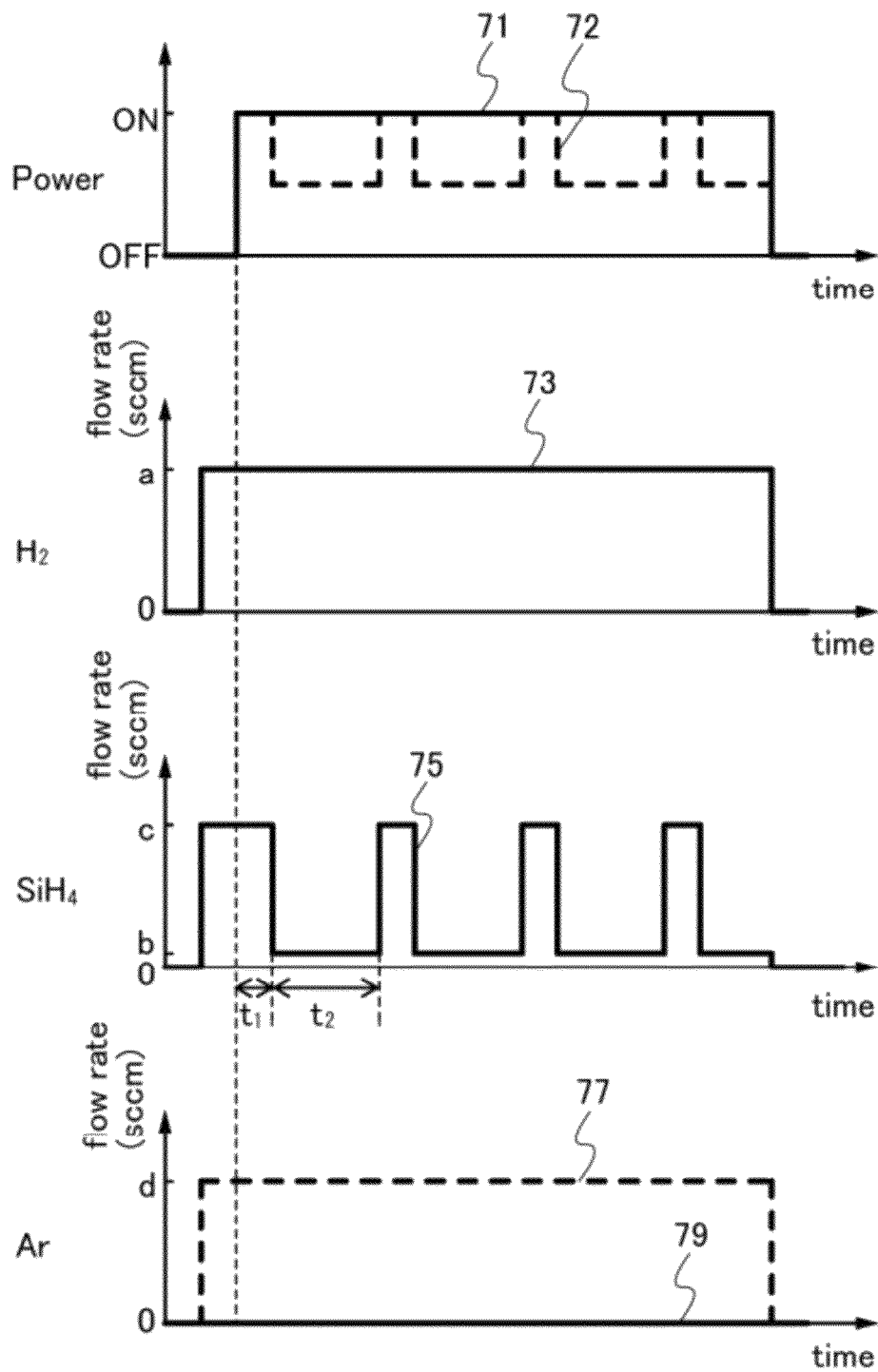


FIG. 3

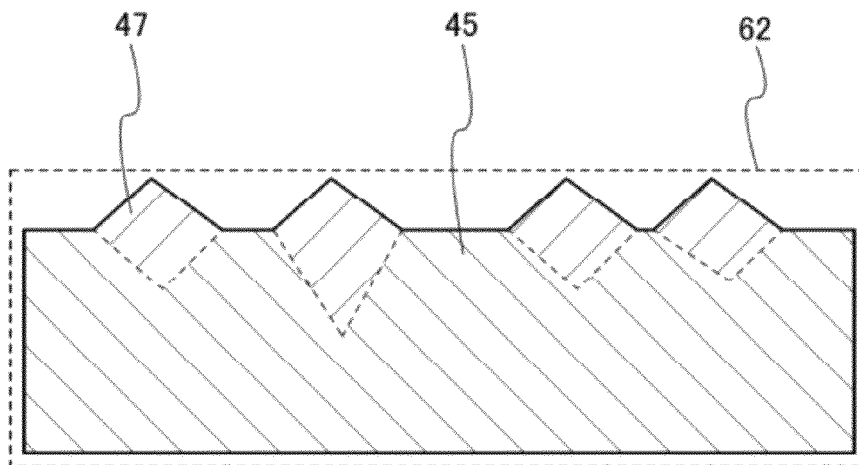


FIG. 4A

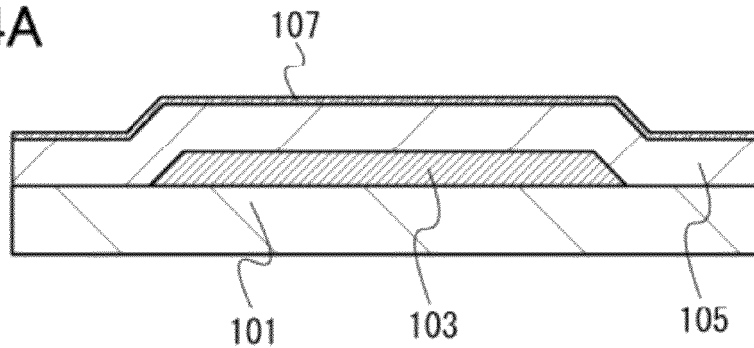


FIG. 4B

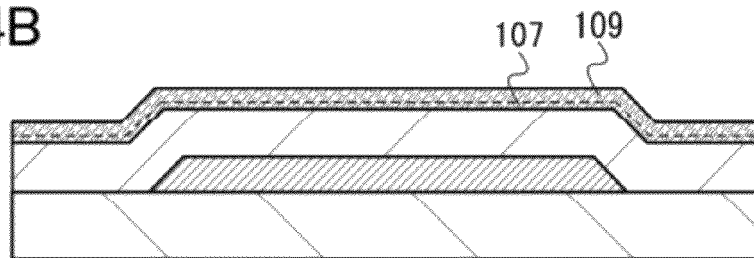


FIG. 4C

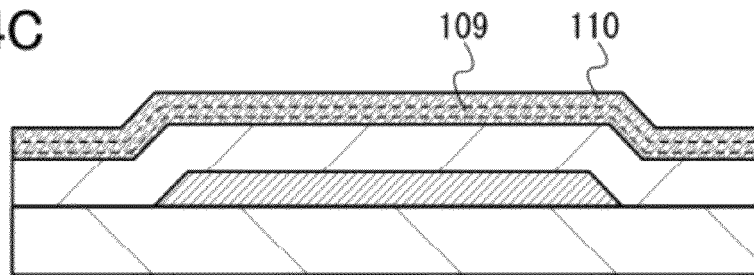


FIG. 4D

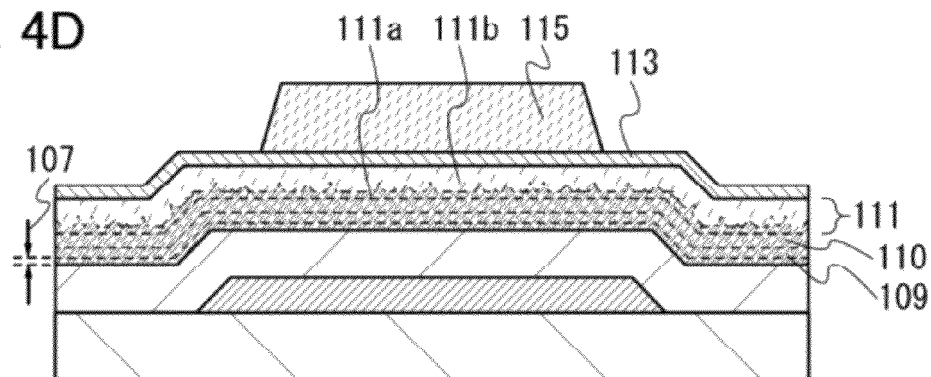


FIG. 4E

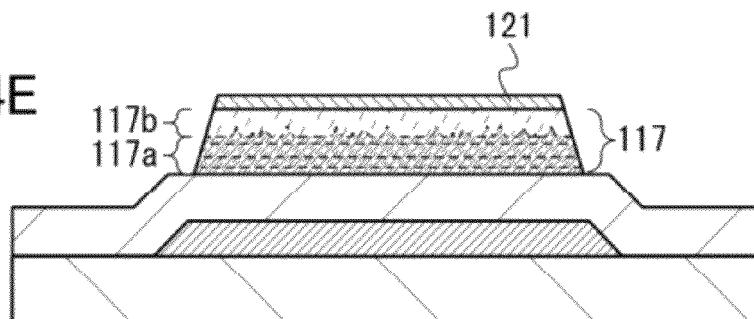


FIG. 5A

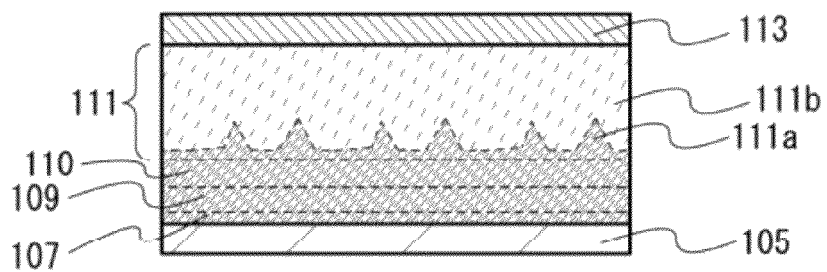


FIG. 5B

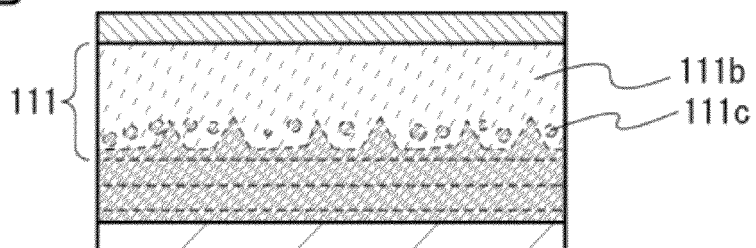


FIG. 6A

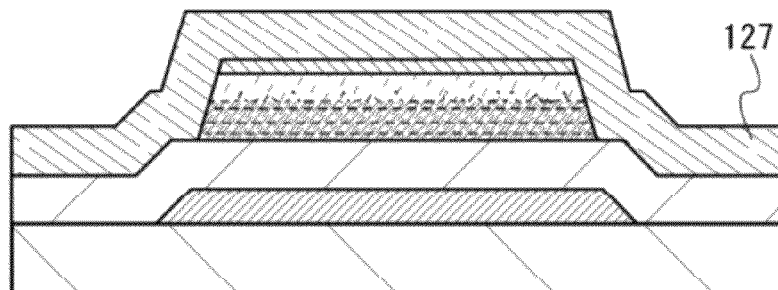


FIG. 6B

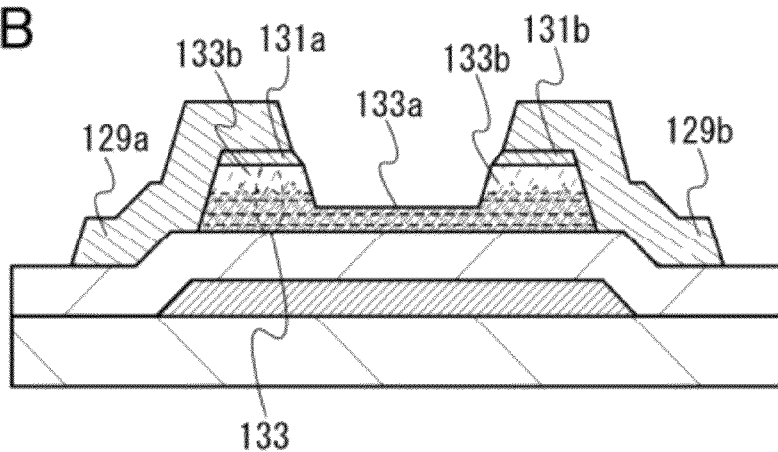


FIG. 6C

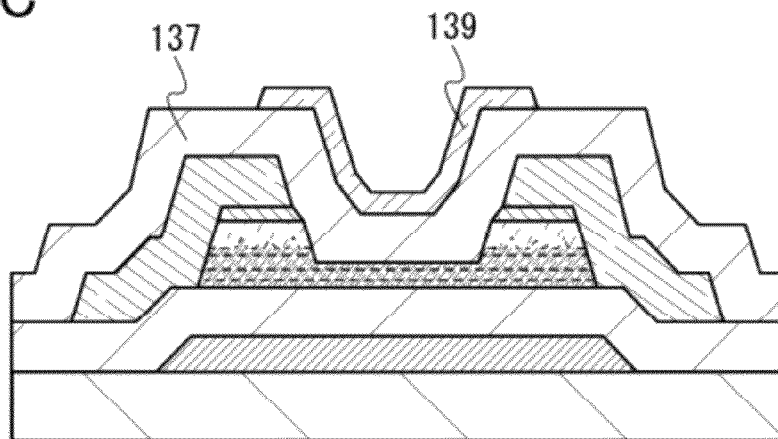


FIG. 7A

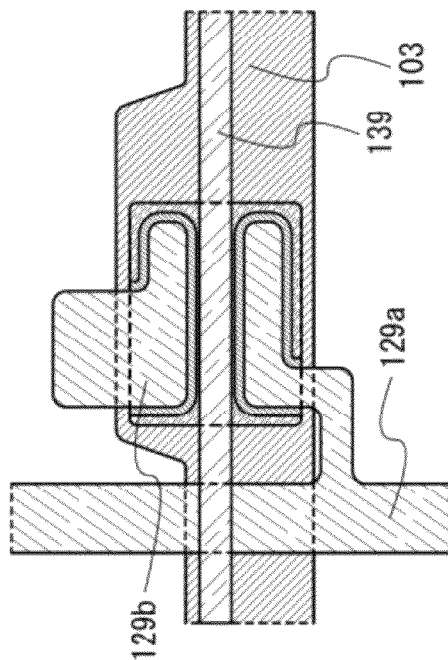


FIG. 7C

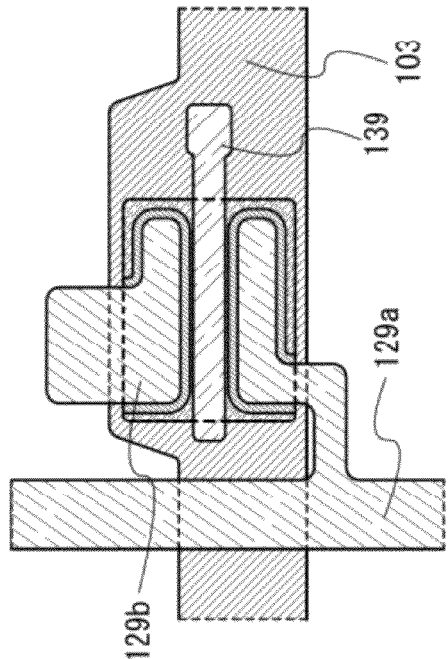


FIG. 7B

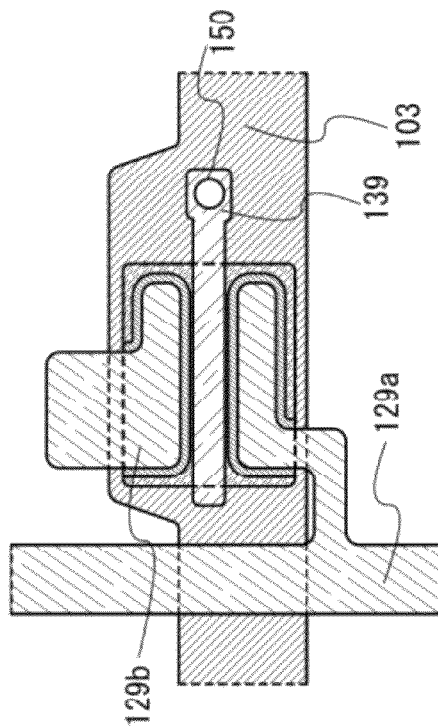


FIG. 7D

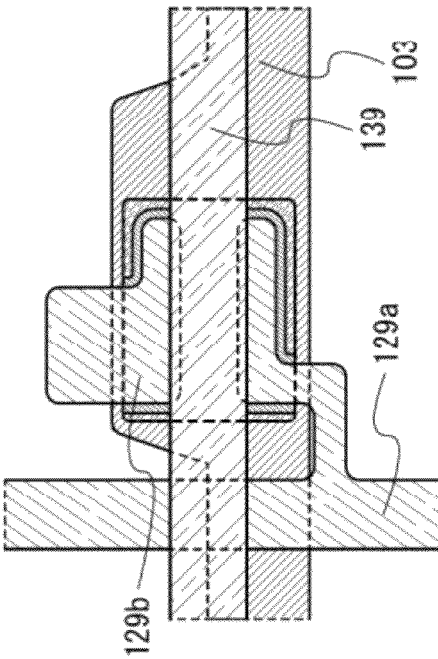


FIG. 8A

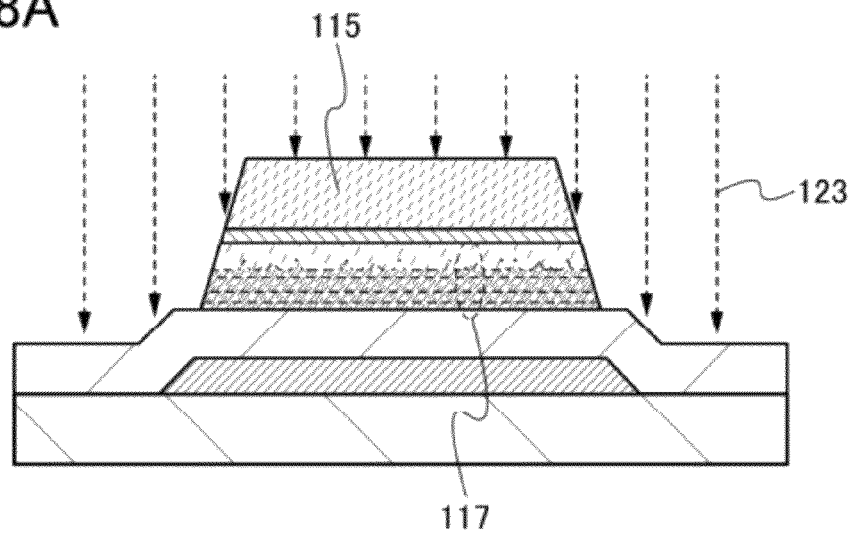


FIG. 8B

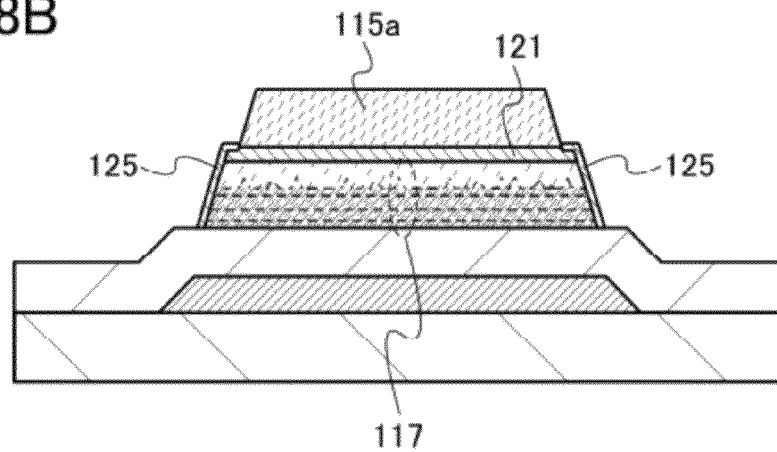


FIG. 8C

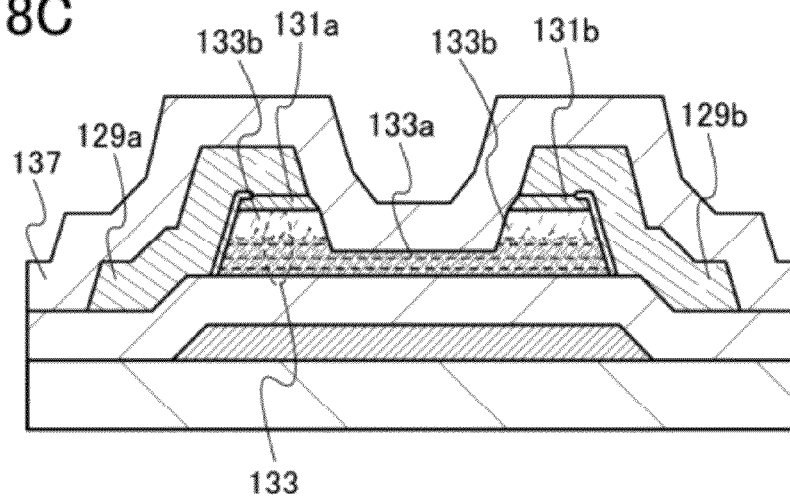


FIG. 9

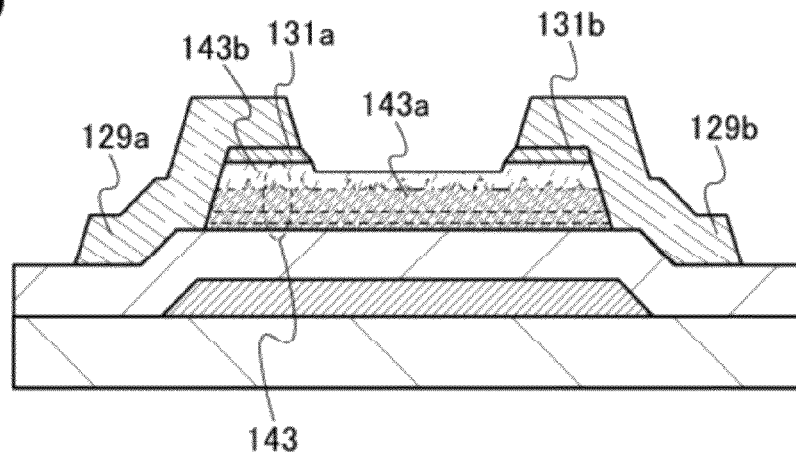


FIG. 10A

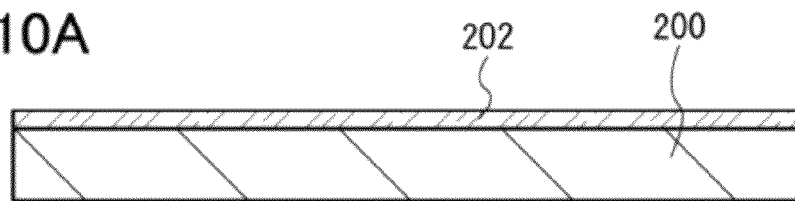


FIG. 10B

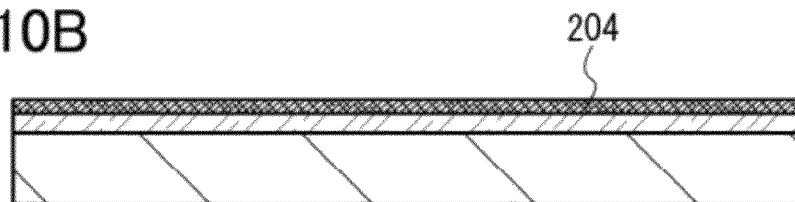


FIG. 10C

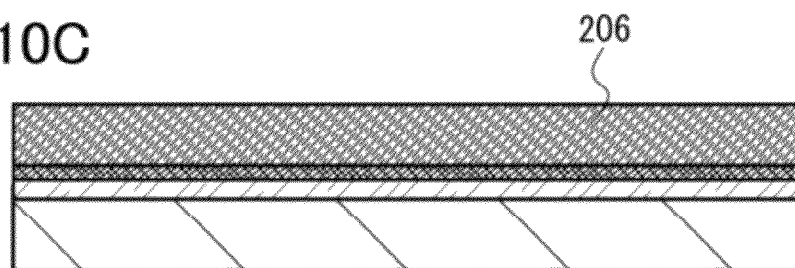


FIG. 10D

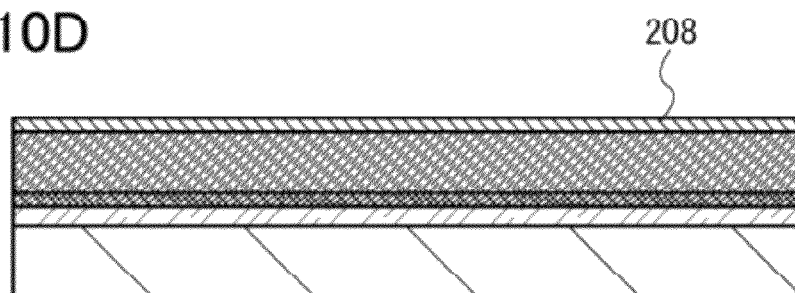


FIG. 10E

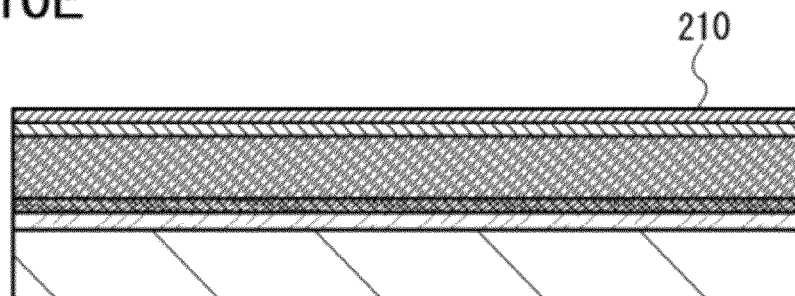


FIG. 11

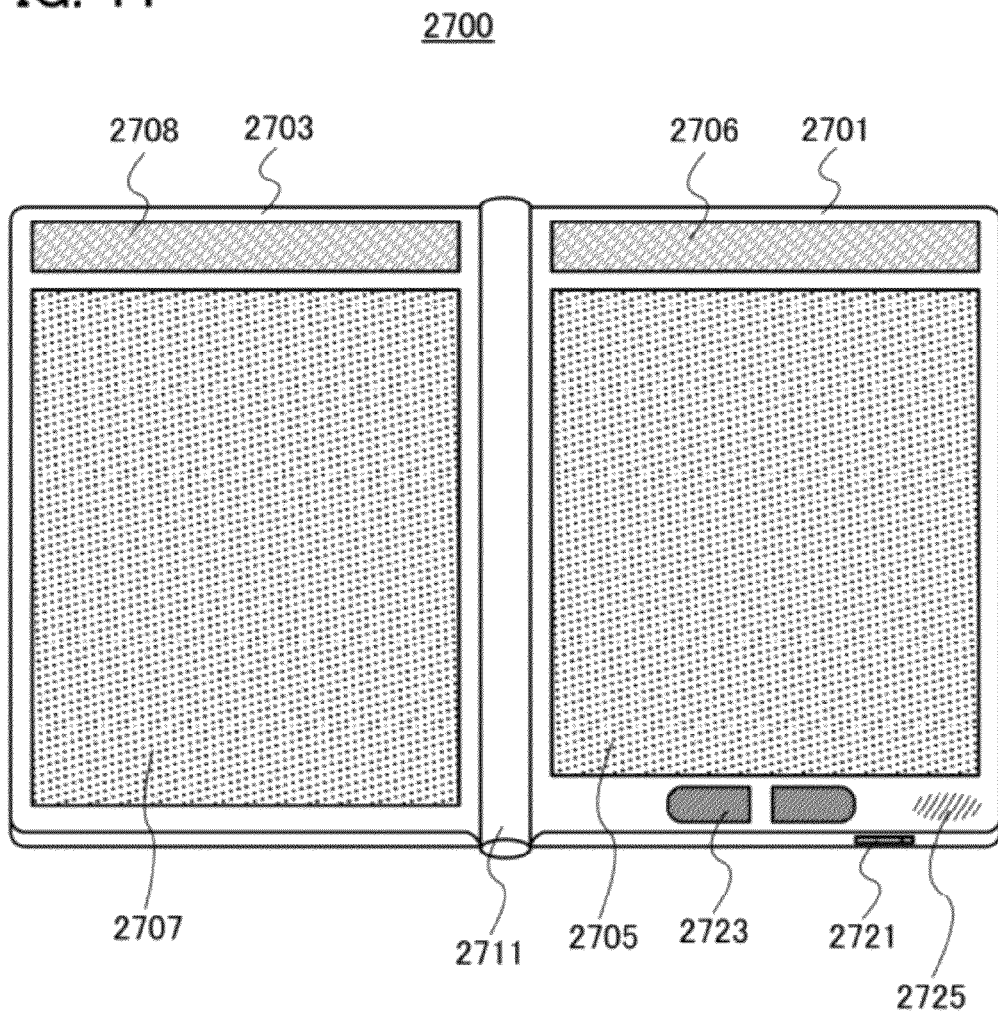


FIG. 12A

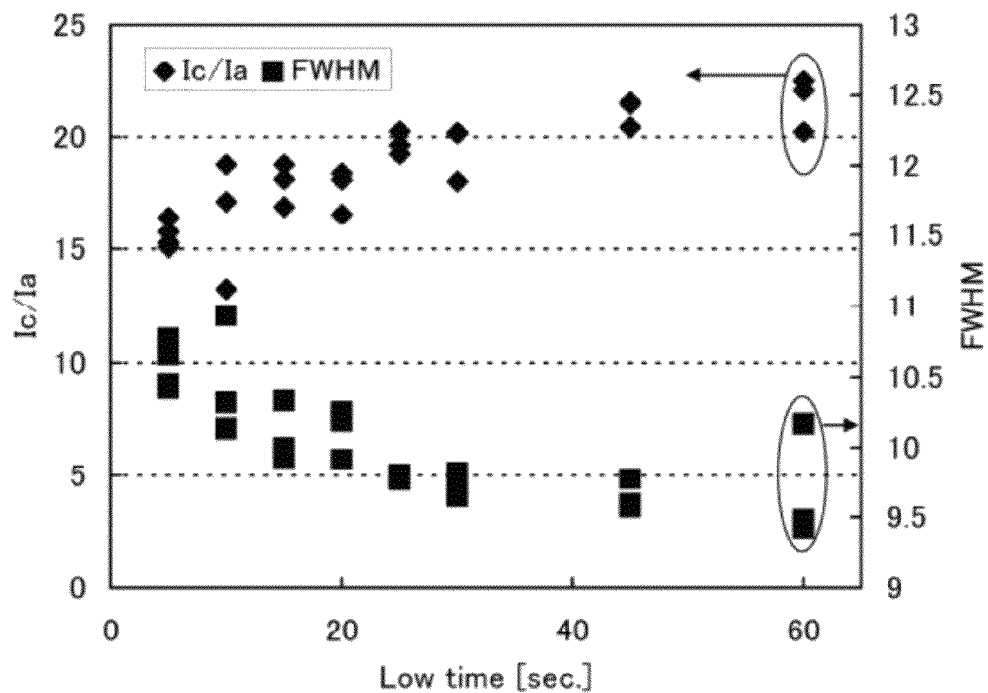


FIG. 12B

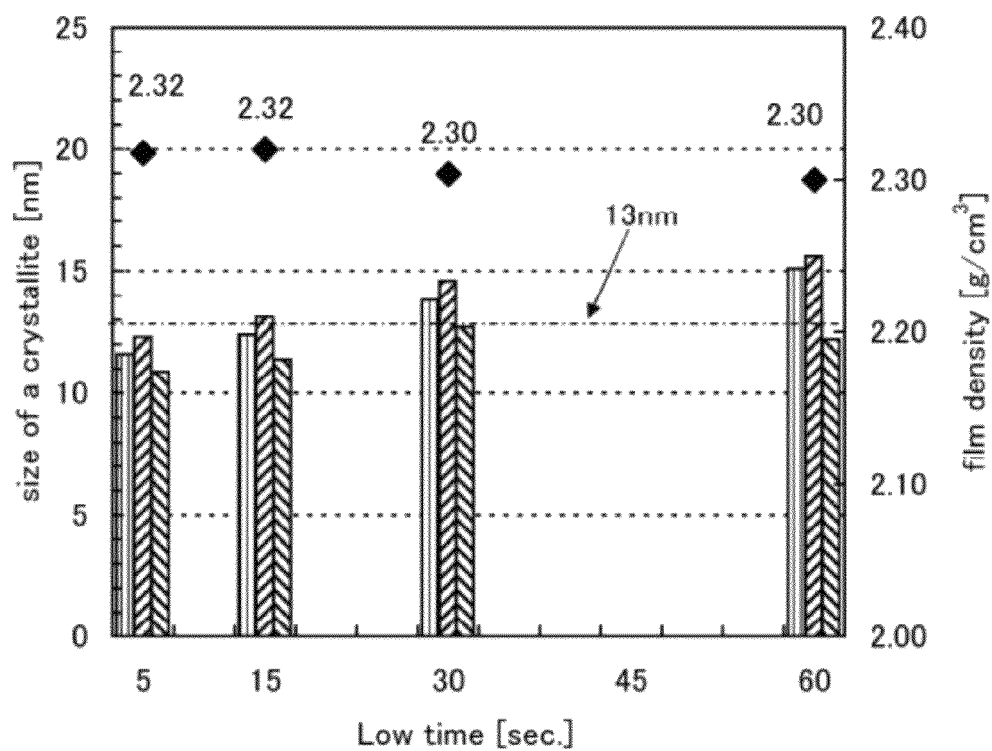


FIG. 13A

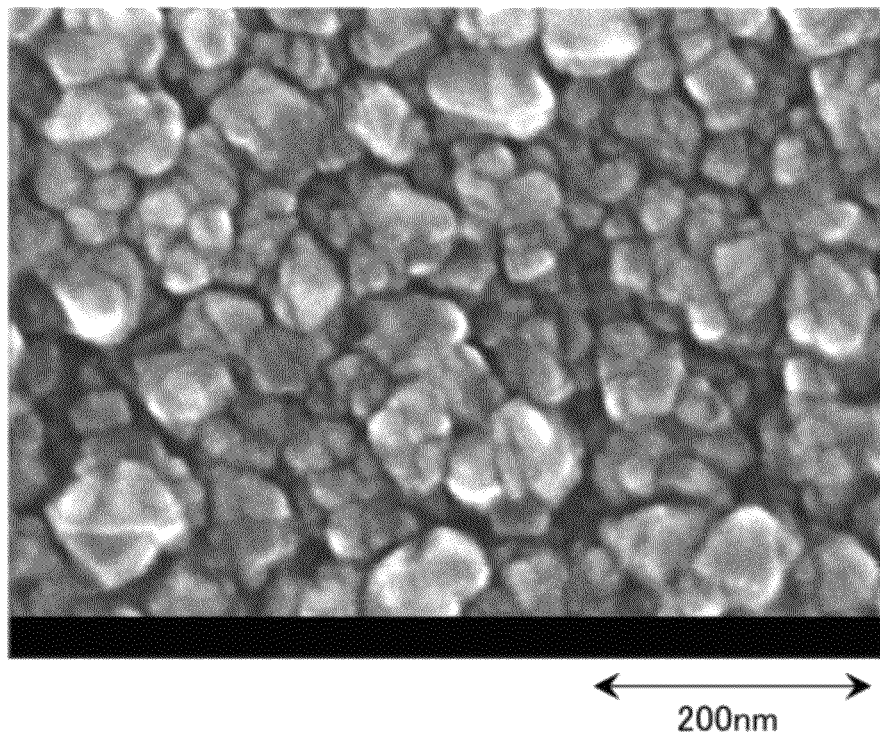


FIG. 13B

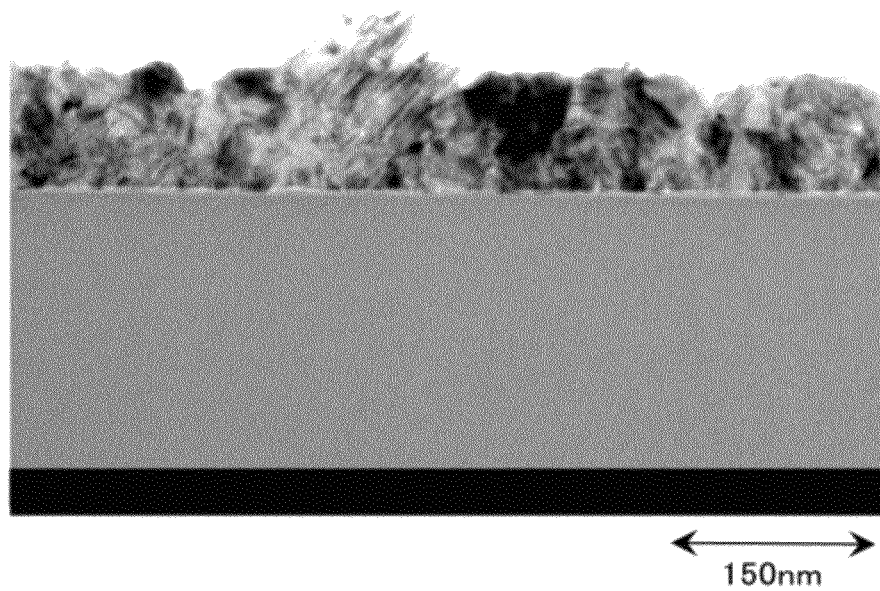


FIG. 14A

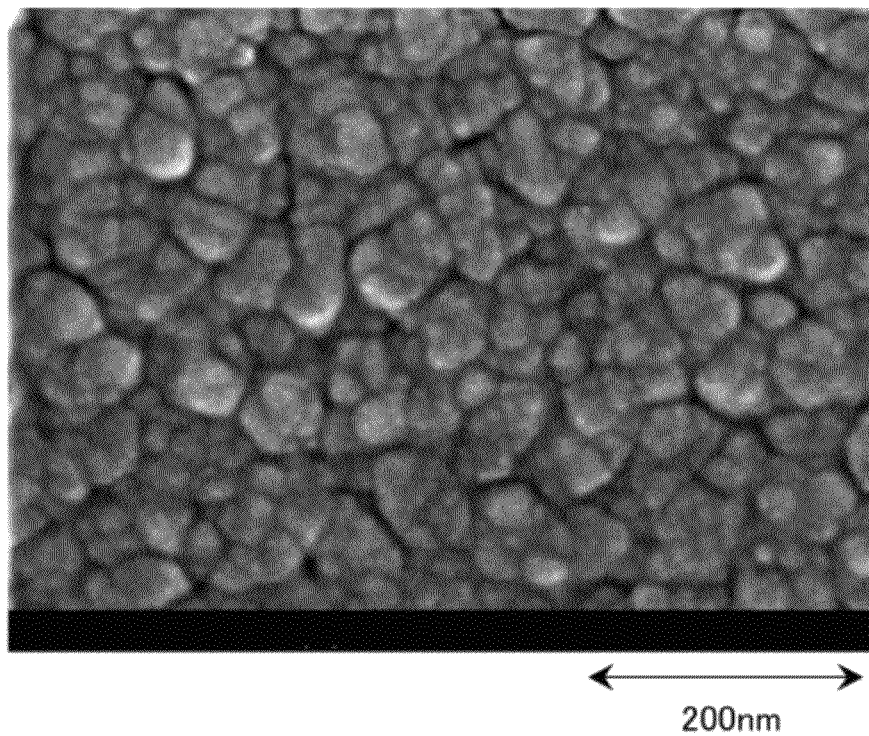


FIG. 14B

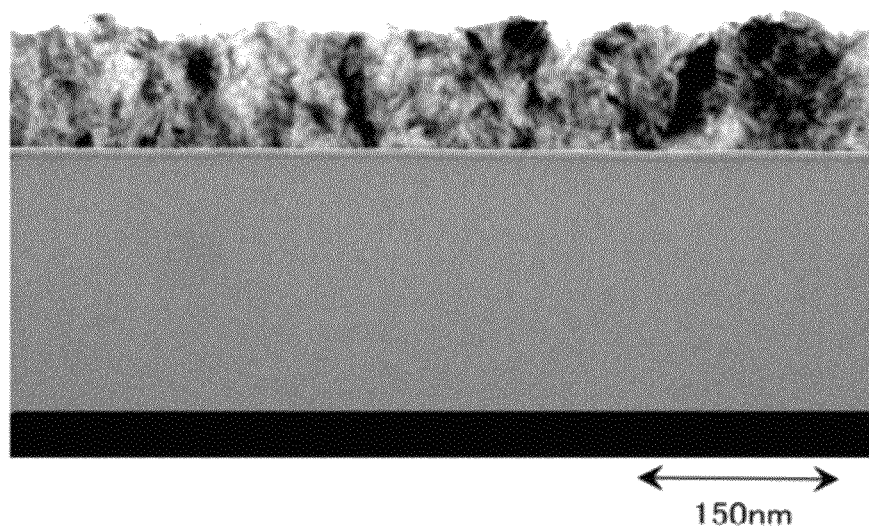
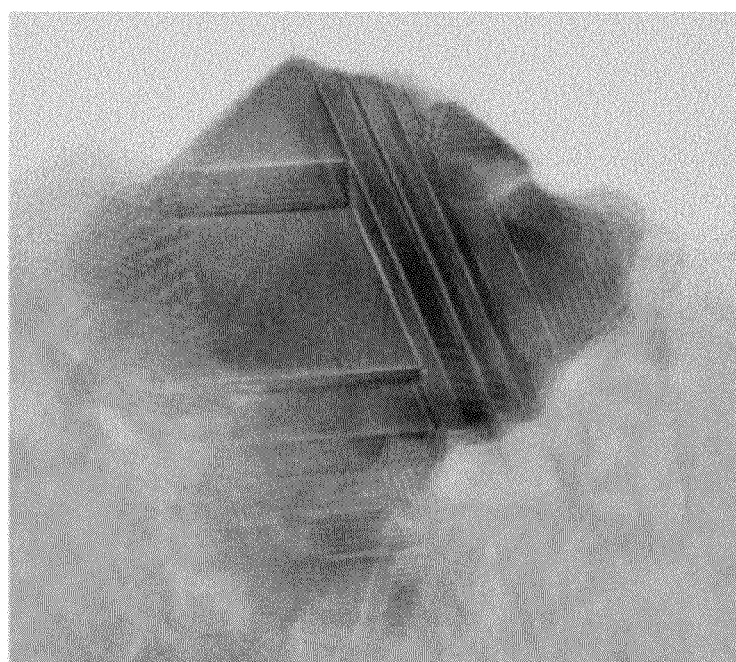


FIG. 15A



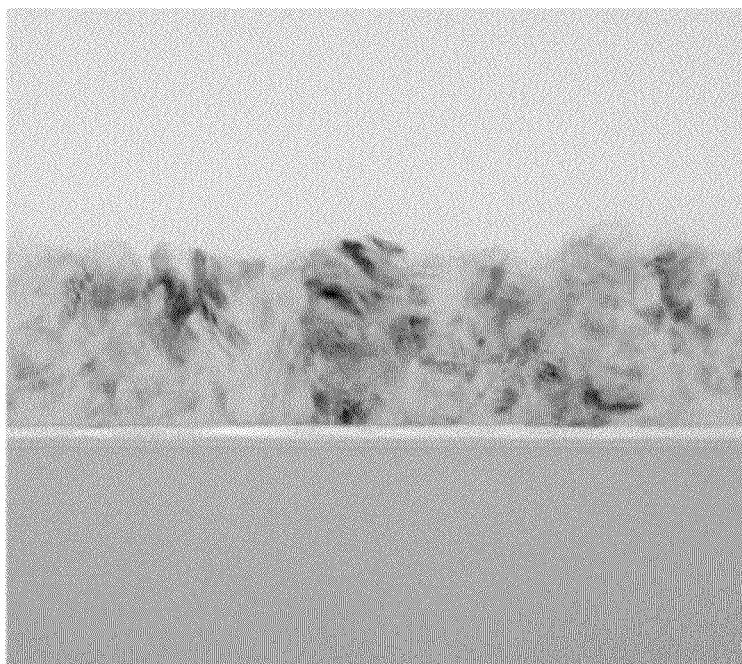
↔
50nm

FIG. 15B



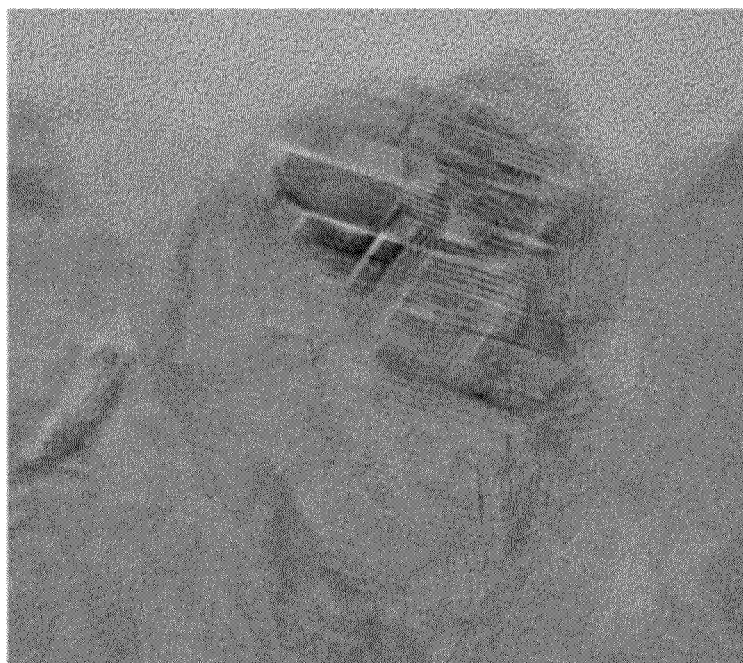
↔
10nm

FIG. 16A



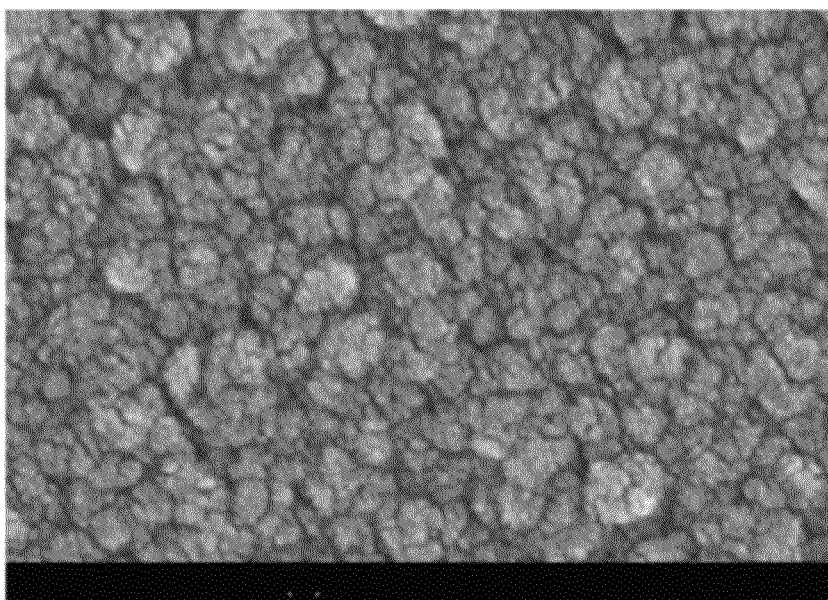
50nm

FIG. 16B



10nm

FIG. 17



200nm

MICROCRYSTALLINE SEMICONDUCTOR FILM, METHOD FOR MANUFACTURING THE SAME, AND METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a microcrystalline semiconductor film, a method for manufacturing the microcrystalline semiconductor film, a method for manufacturing a semiconductor device including the microcrystalline semiconductor film, and a display device.

In this specification, a semiconductor device means all types of devices which can function by utilizing semiconductor characteristics, and a display device, an electro-optical device, a photoelectric conversion device, a semiconductor circuit, and an electronic device are all semiconductor devices.

2. Description of the Related Art

As one type of field-effect transistor, a thin film transistor whose channel region is formed in a semiconductor film which is formed over a substrate having an insulating surface is known. Techniques in which amorphous silicon, microcrystalline silicon, or polycrystalline silicon is used for the semiconductor film where the channel region is formed in the thin film transistor have been disclosed (see Patent Documents 1 to 5). A typical application of the thin film transistor is a liquid crystal television device, in which the thin film transistor is practically used as a switching transistor in each pixel in a display screen.

In addition, a photoelectric conversion device has been developed in which a microcrystalline silicon film, which is a film of crystalline silicon capable of being formed by a plasma CVD method, is used as a semiconductor film having a function of photoelectric conversion (for example, see Patent Document 6).

[Reference]

[Patent Document]

[Patent Document 1] Japanese Published Patent Application No. 2001-053283

[Patent Document 2] Japanese Published Patent Application No. H5-129608

[Patent Document 3] Japanese Published Patent Application No. 2005-049832

[Patent Document 4] Japanese Published Patent Application No. H7-131030

[Patent Document 5] Japanese Published Patent Application No. 2005-191546

[Patent Document 6] Japanese Published Patent Application No. 2000-277439

SUMMARY OF THE INVENTION

A thin film transistor whose channel region is formed using an amorphous silicon film has problems of low field-effect mobility and low on-state current. On the other hand, a thin film transistor whose channel region is formed using a microcrystalline silicon film has such a problem that, though the field-effect mobility is improved, the off-state current is high as compared to the thin film transistor whose channel region is formed using an amorphous silicon film and thus sufficient switching characteristics cannot be obtained.

A thin film transistor whose channel region is formed using a polycrystalline silicon film has a field-effect mobility much higher than and on-state current higher than those of the

above two kinds of thin film transistors. These features enable this kind of thin film transistor to be used not only as a switching transistor in a pixel but also as an element of a driver circuit that needs high-speed operation.

However, a manufacturing process of the thin film transistor whose channel region is formed using a polycrystalline silicon film involves a crystallization step for a semiconductor film and has a problem of higher manufacturing costs as compared to a manufacturing process of the thin film transistor whose channel region is formed using an amorphous silicon film. For example, a laser annealing technique necessary in the process for forming a polycrystalline silicon film prohibits efficient production of large-screen liquid crystal panels because an irradiation area of the laser beam is small.

The size of a glass substrate for manufacturing display panels has grown as follows: the 3rd generation (550 mm×650 mm), the 3.5th generation (600 mm×720 mm or 620 mm×750 mm), the 4th generation (680 mm×880 mm or 730 mm×920 mm), the 5th generation (1100 mm×1300 mm), the 6th generation (1500 mm×1850 mm), the 7th generation (1870 mm×2200 mm), the 8th generation (2200 mm×2400 mm), the 9th generation (2400 mm×2800 mm), and the 10th generation (2950 mm×3400 mm). The increase in size of glass substrate is based on the concept of minimum cost design.

However, a technique has not been established yet with which thin film transistors capable of high-speed operation can be manufactured with high productivity over a large-sized mother glass substrate such as the 10th generation mother glass substrate (2950 mm×3400 mm), which is a problem in the industry.

An object of an embodiment of the present invention is to provide a microcrystalline semiconductor film having high crystallinity and a manufacturing method thereof. Another object of an embodiment of the present invention is to provide a method for manufacturing a semiconductor device having favorable electrical characteristics with high productivity.

An embodiment of the present invention is a microcrystalline semiconductor film having a thickness of more than or equal to 70 nm and less than or equal to 100 nm and including a crystal grain part of which projects from a surface of the microcrystalline semiconductor film. The crystal grain has an orientation plane and includes a crystallite having a size of 13 nm or more. Further, the film density of the microcrystalline semiconductor film is higher than or equal to 2.25 g/cm³ and lower than or equal to 2.35 g/cm³, preferably higher than or equal to 2.30 g/cm³ and lower than or equal to 2.33 g/cm³. Note that the above-mentioned crystal grain is also referred to as a mixed phase grain. The mixed phase grain includes an amorphous semiconductor region and a crystallite which is a microcrystal that can be regarded as a single crystal. In some cases, the mixed phase grain may include a twin crystal. Accordingly, the microcrystalline semiconductor film includes an amorphous semiconductor region. Further, since the microcrystalline semiconductor film includes mixed phase grains, many crystallites are included in the microcrystalline semiconductor film.

The size of the crystallite is the value obtained by substituting the full width at half maximum of a peak indicating the orientation in the spectrum measured by X-ray diffraction, into the Scherrer Equation, and is the average size of a single crystal having an orientation in the microcrystalline semiconductor film.

One feature of an embodiment of the present invention is that, after forming a seed crystal including high-crystallinity mixed phase grains at a low grain density over an insulating film under a first condition, a first microcrystalline semicon-

ductor film is formed on the seed crystal under a second condition so as to grow the mixed phase grains and fill a space between the mixed phase grains, and then a microcrystalline semiconductor film having high crystallinity is formed on the first microcrystalline semiconductor film under a third condition without increasing the space between the mixed phase grains included in the first microcrystalline semiconductor film.

The first condition that allows formation of high-crystallinity mixed phase grains at a low density is a condition that a deposition gas containing silicon or germanium is diluted so that the flow rate of hydrogen is more than or equal to 50 times and less than or equal to 1000 times that of the deposition gas and the pressure in a process chamber is higher than or equal to 67 Pa and lower than or equal to 50000 Pa, preferably higher than or equal to 67 Pa and lower than or equal to 13332 Pa. The second condition that allows the mixed phase grains to grow and the space between the mixed phase grains to be filled is a condition that a deposition gas containing silicon or germanium is diluted so that the flow rate of hydrogen is more than or equal to 100 times and less than or equal to 2000 times that of the deposition gas and the pressure in a process chamber is higher than or equal to 1333 Pa and lower than or equal to 50000 Pa, preferably higher than or equal to 1333 Pa and lower than or equal to 13332 Pa.

The third condition that allows formation of a microcrystalline semiconductor film having high crystallinity without increasing the space between the mixed phase grains included in the first microcrystalline semiconductor film is a condition that the pressure in a process chamber is higher than or equal to 1333 Pa and lower than or equal to 50000 Pa, preferably higher than or equal to 1333 Pa and lower than or equal to 13332 Pa, and a first period in which microcrystalline semiconductor is deposited and a second period that is longer than the first period, in which an amorphous semiconductor region included in the microcrystalline semiconductor is selectively etched, are performed alternately.

Another embodiment of the present invention is a method in which a seed crystal which includes a mixed phase grain including an amorphous semiconductor region and a crystallite which is a microcrystal that can be regarded as a single crystal is formed by a plasma CVD method under a first condition, a first microcrystalline semiconductor film is formed over the seed crystal by a plasma CVD method under a second condition, and a second microcrystalline semiconductor film is formed over the first microcrystalline semiconductor film under a third condition. The first condition is a condition that a deposition gas containing silicon or germanium and a gas containing hydrogen are used as source gas supplied to a process chamber, the deposition gas is diluted so that the flow rate of hydrogen is more than or equal to 50 times and less than or equal to 1000 times that of the deposition gas, and the pressure in the process chamber is higher than or equal to 67 Pa and lower than or equal to 50000 Pa, preferably higher than or equal to 67 Pa and lower than or equal to 13332 Pa. The second condition is a condition that a deposition gas containing silicon or germanium is diluted so that the flow rate of hydrogen is more than or equal to 100 times and less than or equal to 2000 times that of the deposition gas and the pressure in a process chamber is higher than or equal to 1333 Pa and lower than or equal to 50000 Pa, preferably higher than or equal to 1333 Pa and lower than or equal to 13332 Pa. The third condition is a condition that the pressure in a process chamber is higher than or equal to 1333 Pa and lower than or equal to 50000 Pa, preferably higher than or equal to 1333 Pa and lower than or equal to 13332 Pa, and a first period in which microcrystalline semiconductor is deposited and a sec-

ond period that is longer than the first period, in which an amorphous semiconductor region included in the microcrystalline semiconductor is selectively etched, are performed alternately.

Note that the seed crystal may be in a state in which a plurality of mixed phase grains are dispersed or in a state in which a plurality of mixed phase grains are continuously provided in a state of having a film shape) in some cases. It is preferable to determine the power for generating plasma as appropriate according to the flow rate ratio of hydrogen to the deposition gas containing silicon or germanium.

Further, in one embodiment of the present invention, a rare gas may be added to the source gas used in at least one of the first condition, the second condition, and the third condition.

According to another embodiment of the present invention, a seed crystal including high-crystallinity mixed phase grains at a low grain density is formed over an insulating film by a plasma CVD method under a first condition, a first microcrystalline semiconductor film is formed on the seed crystal by a plasma CVD method under a second condition so as to grow the mixed phase grains and fill a space between the mixed phase grains, and then a microcrystalline semiconductor film having high crystallinity is formed on the first microcrystalline semiconductor film by a plasma CVD method under a third condition without increasing the space between the mixed phase grains included in the first microcrystalline semiconductor film.

Another embodiment of the present invention is a method, for manufacturing a semiconductor device including a thin film transistor whose channel region is formed using a microcrystalline semiconductor film in which the seed crystal, the first microcrystalline semiconductor film, and the second microcrystalline semiconductor film are stacked.

Another embodiment of the present invention is a method for manufacturing a photoelectric conversion device in which the microcrystalline semiconductor film which the seed crystal, the first microcrystalline semiconductor film, and the second microcrystalline semiconductor film are stacked is used as at least one of a semiconductor film having p-type conductivity, a semiconductor film having n-type conductivity, and a semiconductor film having a function of photoelectric conversion.

According to one embodiment of the present invention, a microcrystalline semiconductor film having high crystallinity can be formed. Further, a semiconductor device having favorable electrical characteristics can be manufactured with high productivity.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIGS. 1A to 1F are cross-sectional views illustrating a method for forming a microcrystalline semiconductor film according to one embodiment of the present invention;

FIG. 2 is a diagram showing a method for forming a microcrystalline semiconductor film according to one embodiment of the present invention;

FIG. 3 is a cross-sectional view illustrating a microcrystalline semiconductor film according to one embodiment of the present invention;

FIGS. 4A to 4E are cross-sectional views illustrating a method for manufacturing a semiconductor device according to one embodiment of the present invention;

FIGS. 5A and 5B are cross-sectional views illustrating a method for manufacturing a semiconductor device according to one embodiment of the present invention;

5

FIGS. 6A to 6C are cross-sectional views illustrating a method for manufacturing a semiconductor device according to one embodiment of the present invention.

FIGS. 7A to 7D are top views each illustrating a method for manufacturing a semiconductor device according to one embodiment of the present invention;

FIGS. 8A to 8C are cross-sectional views illustrating a method for manufacturing a semiconductor device according to one embodiment of the present invention;

FIG. 9 is a cross-sectional view illustrating a method for manufacturing a semiconductor device according to one embodiment of the present invention;

FIGS. 10A to 10E are cross-sectional views illustrating one embodiment of a method for manufacturing a photoelectric conversion device;

FIG. 11 is a perspective view illustrating an example of an e-book reader;

FIG. 12A shows results of Raman spectroscopic analysis of microcrystalline semiconductor films and FIG. 12B shows evaluation results by an in-plane X-ray diffraction method and evaluation results by X-ray reflectometry;

FIGS. 13A and 13B are SEM photographs of a microcrystalline semiconductor film;

FIGS. 14A and 14B are SEM photographs of a microcrystalline semiconductor film;

FIGS. 15A and 15B are TEM photographs of a microcrystalline semiconductor film;

FIGS. 16A and 16B are TEM photographs of a microcrystalline semiconductor film; and

FIG. 17 is a SEM photograph of a microcrystalline semiconductor film.

DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, embodiments and an example of the present invention will be described with reference to the drawings. Note that the present invention is not limited to the following description. It will be readily appreciated by those skilled in the art that the mode and details can be changed in various different ways without departing from the spirit and the scope of the present invention. Therefore, the present invention should not be construed as being limited to the following description of the embodiments and example. Note that the same reference numerals are commonly used to denote the same components among different drawings. (Embodiment 1)

In this embodiment, a method for forming a microcrystalline semiconductor film in which the crystallinity is improved by reduction of a space between mixed phase grains will be described with reference to FIGS. 1A to 1F and FIG. 2.

As illustrated in FIG. 1A, an insulating film 55 is formed over a substrate 51, and a seed crystal 57 is formed over the insulating film. 55.

As the substrate 51, a glass substrate, a ceramic substrate, a plastic substrate which has heat resistance enough to withstand a process temperature of this manufacturing process, or the like can be used. In the case where the substrate does not need a light-transmitting property, a metal substrate, such as a stainless steel substrate, provided with an insulating film on its surface may be used. As the glass substrate, for example, an alkali-free glass substrate of barium borosilicate glass, aluminoborosilicate glass, aluminosilicate glass, or the like may be used. Note that there is no limitation on the size of the substrate 51. For example, any of glass substrates of the 3rd to 10th generations which are often used in the field of the above flat panel displays can be used.

6

The insulating film 55 can be formed as a single layer or a stacked layer using a silicon oxide film, a silicon oxynitride film, a silicon nitride film, a silicon nitride oxide film, an aluminum oxide film, an aluminum nitride film, an aluminum oxynitride film, or an aluminum nitride oxide film by a CVD method, a sputtering method, or the like.

Note that here, silicon oxynitride contains more oxygen than nitrogen. In the case where measurements are performed using Rutherford backscattering spectrometry

(RBS) and hydrogen forward scattering spectrometry (1-IFS), silicon oxynitride preferably contains oxygen, nitrogen, silicon, and hydrogen at 50 at. % to 70 at. %, 0.5 at. % to 15 at. %, 25 at. % to 35 at. %, and 0.1 at. % to 10 at. %, respectively. Further, silicon nitride oxide contains more nitrogen than oxygen. In the case where measurements are performed using RBS and HFS, silicon nitride oxide preferably contains oxygen, nitrogen, silicon, and hydrogen at 5 at. % to 30 at. %, 20 at. % to 55 at. %, 25 at. % to 35 at. %, and 10 at. % to 30 at. %, respectively. Note that percentages, of nitrogen, oxygen, silicon, and hydrogen fall within the ranges given above, where the total number of atoms contained in the silicon oxynitride or the silicon nitride oxide is defined as 100 at. %.

The seed crystal 57 is formed using microcrystalline semiconductor typified by microcrystalline silicon, microcrystalline silicon germanium, microcrystalline germanium, or the like. The seed crystal 57 may be in a state in which a plurality of mixed phase grains is dispersed, in a state in which mixed phase grains are continuously provided and form a film, or in a state in which mixed phase grains and an amorphous semiconductor region are continuously provided and form a film. Therefore, the seed crystal 57 may have a space 57b between adjacent mixed phase grains 57a without the mixed phase grains 57a and/or the amorphous semiconductors being in contact with each other. Further, a feature of the seed crystal 57 is such that the density of the mixed phase grains (the existing proportion of the mixed phase grains in a plane) is low and the crystallinity of the mixed phase grains is high.

The seed crystal 57 is formed in a process chamber of a plasma CVD apparatus by glow discharge plasma using a mixture of hydrogen and a deposition gas containing silicon or germanium, under a first condition that enables mixed phase grains having high crystallinity to be formed at a low density. Alternatively, the seed crystal 57 is formed by glow discharge plasma using a mixture of hydrogen, a deposition gas containing silicon or germanium, and a rare gas such as helium, neon, argon, krypton, or xenon. Here, microcrystalline silicon, microcrystalline silicon germanium, microcrystalline germanium, or the like is deposited as the seed crystal 57 under the first condition that the deposition gas is diluted so that the flow rate of hydrogen is more than or equal to 50 times and less than or equal to 1000 times that of the deposition gas containing silicon or germanium, and the pressure in the process chamber is higher than or equal to 67 Pa and lower than or equal to 50000 Pa (higher than or equal to 0.5 Torr and lower than or equal to 370 Torr), preferably higher than or equal to 67 Pa and lower than or equal to 13332 Pa (higher than or equal to 0.5 Torr and lower than or equal to 100 Torr). At this time, the deposition temperature is preferably room temperature to 350° C., further preferably 150° C. to 280° C. The distance between an upper electrode and a lower electrode in the process chamber is set to a distance that enables generation of plasma. With the first condition, crystal growth is promoted and the crystallinity of the mixed phase grains 57a in the seed crystal 57 is improved. In other words, the size of the crystallites included in the mixed phase grains 57a in the seed crystal 57 is increased. Further, the space 57b is

formed between the adjacent mixed phase grains **57a**, which leads to a low density of the mixed phase grains **57a**. Note that in the above-description of the flow rate of hydrogen and the flow rate of the deposition gas containing silicon or germanium, the deposition gas containing silicon or germanium means a 100% undiluted deposition gas containing silicon or germanium. Accordingly, in the case where the deposition gas containing silicon or germanium is diluted, the flow rate of the 100% deposition gas containing silicon or germanium in the diluted gas is calculated and then the flow rate of hydrogen is adjusted based on the flow rate of the 100% deposition gas.

As typical examples of the deposition gas containing silicon or germanium, there are SiH_4 , Si_2H_6 , GeH_4 , Ge_2H_6 , and the like.

When a rare gas such as helium, neon, argon, krypton, or xenon is added to the source gas of the seed crystal **57**, the deposition rate of the seed crystal **57** is increased, which can reduce the amount of impurities mixed in the seed crystal **57**. Accordingly, the crystallinity of the seed crystal **57** can be improved. By adding a rare gas such as helium, neon, argon, krypton, or xenon to the source gas of the seed crystal **57**, stable plasma generation is possible without application of high power. Therefore, plasma damage to the seed crystal **57** can be reduced and the crystallinity of the seed crystal **57** can be improved.

When the seed crystal **57** is formed, glow discharge plasma is generated by application of high-frequency power with a frequency of 3 MHz to 30 MHz, typically 13.56 MHz or 27.12 MHz in the HF band, or high-frequency power with a frequency of approximately 30 MHz to 300 MHz in the VHF band, typically 60 MHz. Alternatively, glow discharge plasma is generated by application of high-frequency power with a microwave of 1 GHz or higher. Note that pulsed oscillation by which high-frequency power is applied in a pulsed manner or continuous oscillation by which high-frequency power is applied continuously can be employed. In addition, by superimposing high-frequency power in the HF band and high-frequency power in the VHF band on each other, unevenness of plasma across a large-sized substrate is also reduced, so that uniformity in film thickness and film quality can be increased and the deposition rate can be increased.

The flow rate of hydrogen is set higher than the flow rate of the deposition gas containing silicon or germanium as described above, whereby the amorphous semiconductor region in the seed crystal **57** is etched while the seed crystal **57** is deposited; thus, the mixed phase grains **57a** having high crystallinity can be formed and the space **57b** can be formed between the adjacent mixed phase grains **57a**. Optimal conditions differ according to an apparatus structure and a chemical state of a surface on which a film is to be formed: if the mixed phase grains **57a** are hardly deposited, the flow rate ratio of hydrogen to the deposition gas containing silicon or germanium may be reduced or the RF electric power may be reduced; on the other hand, if the grain density of the mixed phase grains **57a** is high or an amorphous semiconductor region is larger than a crystalline semiconductor region, the flow rate ratio of hydrogen to the deposition gas containing silicon or germanium may be increased or the RF electric power may be increased. The state of deposition of the seed crystal **57** can be evaluated by scanning electron microscopy (SEM) and Raman spectroscopy. By employing the above conditions of the flow rate ratio and the pressure in the process chamber, the seed crystal **57** can have favorable crystallinity and have a suitable space between the mixed phase grains **57a**. Thus, the mixed phase grains **57a** are formed while the amorphous semiconductor region in the seed crystal **57** is

etched. Accordingly, crystal growth is promoted and the crystallinity of the mixed phase grains **57a** is improved. That is, the size of the crystallites in the mixed phase grains **57a** is increased. Further, since the amorphous semiconductor region between the adjacent mixed phase grains **57a** is etched, the space **57b** is formed between the adjacent mixed phase grains **57a**; accordingly, the mixed phase grains **57a** are formed at a low grain density. Note that when the seed crystal **57** is formed under the first condition of this embodiment, the grain sizes of the mixed phase grains **57a** are uneven in some cases.

Then, as illustrated in FIG. 1B, a first microcrystalline semiconductor film **59** is formed on the seed crystal **57**. The first microcrystalline semiconductor film **59** is formed under a condition that enables crystallites of the seed crystal **57** to grow so that the space between the mixed phase grains is filled.

The first microcrystalline semiconductor film **59** is formed under a second condition in a process chamber of the plasma CVD apparatus by glow discharge plasma using a mixture of hydrogen and a deposition gas containing silicon or germanium. Alternatively, the first microcrystalline semiconductor film **59** may be formed by glow discharge plasma using a mixture of a source gas of the second condition and a rare gas such as helium, neon, argon, krypton, or xenon. Here, the second condition is a condition that the deposition gas containing silicon or germanium is diluted so that the flow rate of hydrogen is more than or equal to 100 times and less than or equal to 2000 times that of the deposition gas, and the pressure inside the process chamber is higher than or equal to 1333 Pa and lower than or equal to 50000 Pa (higher than or equal to 10 Torr and lower than or equal to 370 Torr), preferably higher than or equal to 1333 Pa and lower than or equal to 13332 Pa (higher than or equal to 10 Torr and lower than or equal to 100 Torr).

As the first microcrystalline semiconductor film **59**, a microcrystalline silicon film, a microcrystalline silicon germanium film, a microcrystalline germanium film, or the like is formed under the above second condition. Therefore, in the first microcrystalline semiconductor film **59**, the ratio of the crystal regions to the amorphous semiconductor region is increased and the space between the crystal regions is reduced, whereby the crystallinity is improved. The deposition temperature at this time is preferably room temperature to 350° C., further preferably 150° C. to 280° C. The distance between an upper electrode and a lower electrode in the process chamber is set to a distance that enables generation of plasma.

The condition for generating glow discharge plasma in the formation of the seed crystal **57** can be employed as appropriate for the formation of the first microcrystalline semiconductor film **59**. In the case where the condition for generating glow discharge plasma in the formation of the seed crystal **57** and that in the formation of the first microcrystalline semiconductor film **59** are the same, throughput can be increased. However, the conditions may be different from each other.

The first microcrystalline semiconductor film **59** is formed under the second condition that enables crystallites of the seed crystal **57** to grow so that the space **57b** between the mixed phase grains **57a** is filled. Typically, in the second condition, the deposition gas containing silicon or germanium is diluted so that the flow rate of hydrogen is more than or equal to 100 times and less than or equal to 2000 times that of the deposition gas, and the pressure in the process chamber is higher than or equal to 1333 Pa and lower than or equal to 50000 Pa (higher than or equal to 10 Torr and lower than or equal to 370 Torr), preferably higher than or equal to 1333 Pa

and lower than or equal to 13332 Pa (higher than or equal to 10 Torr and lower than or equal to 100 Torr). Note that in the above-description of the flow rate of hydrogen and the flow rate of the deposition gas containing silicon or germanium, the deposition gas containing silicon or germanium means a 100% undiluted deposition gas containing silicon or germanium. Accordingly, in the case where the deposition gas containing silicon or germanium is diluted, the flow rate of the 100% deposition gas containing silicon or germanium in the diluted gas is calculated and then the flow rate of hydrogen is adjusted based on the flow rate of the 100% deposition gas. Because of such high pressure in the process chamber in the above-described second condition, the mean free path of the deposition gas is short; thus, hydrogen radicals and hydrogen ions lost energy every time they collide with each other. Accordingly, the energy of hydrogen radicals and hydrogen ions becomes lower, which leads to improvement of the coverage and reduction of ion damage, contributing to reduction of defects. Further, in the above condition, since the dilution ratio of the deposition gas containing silicon or germanium is high and the amount of generated hydrogen radicals is increased, the crystal grows using the crystallites in the mixed phase grains **57a** as a nucleus while the amorphous semiconductor region is etched. As a result, in the first microcrystalline semiconductor film **59**, the ratio of the crystal regions to the amorphous semiconductor region is increased and the crystallinity is improved. Further, defects caused in the first microcrystalline semiconductor film **59** during the deposition are reduced.

When mixed phase grains of the first microcrystalline semiconductor film **59** are newly generated in the space **57b** between the mixed phase grains **57a** of the seed crystal **57**, the size of the mixed phase grains of the first microcrystalline semiconductor film **59** becomes smaller. Therefore, it is preferable that the frequency of generation of the mixed phase grains of the first microcrystalline semiconductor film **59** be lower than that of the mixed phase grains **57a** of the seed crystal **57**. In this manner, using the crystallites included in the mixed phase grains **57a** of the seed crystal **57** as nuclei, crystal growth from the seed crystal **57** can be promoted primarily.

Crystal growth of the first microcrystalline semiconductor film **59** occurs using the crystallites in the mixed phase grains **57a** of the seed crystal **57** as nuclei. Further, the size of the mixed phase grain of the first microcrystalline semiconductor film **59** depends on the space between the mixed phase grains **57a** of the seed crystal **57**. Therefore, when the grain density of the mixed phase grains **57a** of the seed crystal **57** is low, the space between the mixed phase grains **57a** is large; thus, the crystal growth distance of the mixed phase grains of the first microcrystalline semiconductor film **59** can be increased and the size of the mixed phase grains in the first microcrystalline semiconductor film **59** can be increased.

Next, as illustrated in FIG. 1C, a second microcrystalline semiconductor film **61** is formed over the first microcrystalline semiconductor film **59**. The second microcrystalline semiconductor film **61** is formed under a condition that allows a microcrystalline semiconductor film having higher crystallinity than the first microcrystalline semiconductor film **59** to be formed without increasing the space between the mixed phase grains included in the first microcrystalline semiconductor film.

The second microcrystalline semiconductor film **61** is formed under a third condition in a process chamber of the plasma CVD apparatus by glow discharge plasma using a mixture of hydrogen and a deposition gas containing silicon or germanium. Alternatively, the second microcrystalline

semiconductor film **61** is formed under a third condition by glow discharge plasma using a mixture of a deposition gas containing silicon or germanium, hydrogen, and a rare gas such as helium, neon, argon, krypton, or xenon. Here, the third condition is a condition that the pressure in the process chamber is higher than or equal to 1333 Pa and lower than or equal to 50000 Pa, preferably higher than or equal to 1333 Pa and lower than or equal to 13332 Pa, and a first period in which microcrystalline semiconductor is deposited and a second period that is longer than the first period, in which an amorphous semiconductor region included in the microcrystalline semiconductor is selectively etched, are performed alternately.

In order to alternately perform the first period for which microcrystalline semiconductor is deposited and the second period that is longer than the first period, in which an amorphous semiconductor region included in the microcrystalline semiconductor is selectively etched, the flow rate ratio of the deposition gas containing silicon or germanium to hydrogen is alternately increased and decreased; specifically, the flow rate of the deposition gas containing silicon or germanium or the flow rate of hydrogen is increased and decreased. In the case where the flow rate ratio of hydrogen to the deposition gas containing silicon or germanium is low, typically, in the case where the flow rate of hydrogen is more than or equal to 100 times and less than or equal to 2000 times that of the deposition gas, deposition and crystal growth of the microcrystalline semiconductor is primarily caused. On the other hand, in the case where the flow rate ratio of hydrogen to the deposition gas containing silicon or germanium is high, typically, in the case where the flow rate of the deposition gas containing silicon or germanium is more than or equal to 0 sccm and less than or equal to 0.3 sccm and the flow rate of hydrogen is more than 1000 sccm, etching of the amorphous semiconductor region included in the microcrystalline semiconductor is primarily caused. Here, in the case where the flow rate of hydrogen is fixed and the flow rate of the deposition gas containing silicon or germanium is increased and decreased, the introduction of the same flow rate of hydrogen as that in the first period to the process chamber enables the pressure in the process chamber to be, constant in the first period and the second period; accordingly, uniformity in the film quality of the second microcrystalline semiconductor film can be increased. In the case where the flow rate ratio of hydrogen to the deposition gas containing silicon or germanium is high, the amorphous semiconductor region is etched primarily rather than the crystallites in the microcrystalline semiconductor at a pressure in the process chamber of higher than or equal to 1333 Pa and lower than or equal to 50000 Pa, further preferably higher than or equal to 1333 Pa and lower than or equal to 13332 Pa. Note that the above-described flow rate ratio of hydrogen to the deposition gas containing silicon or germanium means the flow rate ratio of hydrogen to the 100% undiluted deposition gas containing silicon or germanium. Accordingly, in the case where the deposition gas containing silicon or germanium is diluted, the flow rate of the 100% deposition gas containing silicon or germanium in the diluted gas is calculated and then the flow rate of hydrogen is adjusted based on the flow rate of the 100% deposition gas.

As the second microcrystalline semiconductor film **61**, a microcrystalline silicon film, a microcrystalline silicon germanium film, a microcrystalline germanium film, or the like is formed under the above third condition. Therefore, in the second microcrystalline semiconductor film **61**, the space between the mixed phase grains of the first microcrystalline semiconductor film **59** is not increased and the crystallinity higher than the first microcrystalline semiconductor film is

11

obtained. The deposition temperature at this time is preferably room temperature to 350° C., further preferably 150° C. to 280° C. The distance between an upper electrode and a lower electrode in the process chamber is set to a distance that enables generation of plasma.

A rare gas such as helium, neon, argon, krypton, or xenon may be added to a source gas of the second microcrystalline semiconductor film 61.

The condition for generating glow discharge plasma in the formation of the seed crystal 57 can be employed as appropriate for the formation of the second microcrystalline semiconductor film 61. In the case where the condition for generating glow discharge plasma in the formation of the seed crystal 57, that in the formation of the first microcrystalline semiconductor film 59, and that in the formation of the second microcrystalline semiconductor film 61 are the same, throughput can be increased. However, the conditions may be different from each other.

Here, a method for alternately increasing and decreasing the flow rate ratio of the deposition gas containing silicon or germanium to hydrogen will be described with reference to FIG. 2. FIG. 2 is a timing chart showing temporal changes of the source gas and the power supplied to an apparatus in the method for forming the second microcrystalline semiconductor film 61 described in this embodiment. In FIG. 2, a solid line 71 indicates on/off states of power supply of the plasma CVD apparatus, a solid line 73 indicates the flow rate of hydrogen, a solid line 75 indicates the flow rate of the deposition gas containing silicon or germanium (Oak is used in FIG. 2), and a solid line 79 indicates the flow rate of a rare gas (argon is used in FIG. 2).

The deposition gas containing silicon or germanium, which is a source gas, and hydrogen are introduced into the process chamber of the plasma CVD apparatus, and the pressure therein is set at a predetermined level. The temperature of the substrate 51 is set at a predetermined temperature. At this time, hydrogen is supplied into the process chamber with a fixed flow rate (flow rate a in FIG. 2).

Next, high-frequency power supply is turned on, and plasma discharge is performed. The deposition gas containing silicon or germanium whose flow rate is alternately increased and decreased is supplied into the process chamber. Here, alternately increasing and decreasing the flow rate ratio of the deposition gas containing silicon or germanium to hydrogen is called cycle flow. In this embodiment, after the power supply is turned on, the first period in which the deposition gas containing silicon or germanium with a flow rate c is supplied for t_1 seconds and the second period in which the deposition gas containing silicon or germanium with a flow rate b ($0 < b < c$) is supplied for t_2 seconds are repeated. Here, one feature is that the t_2 seconds of the second period is longer than the t_1 seconds of the first period. The flow rate of the deposition gas containing silicon or germanium in the second period is lower than that in the first period, so that the flow rate ratio of hydrogen to the deposition gas containing silicon or germanium in the second period is higher than that in the first period. In the first period, in the case where the flow rate of hydrogen is made more than or equal to 100 times and less than or equal to 2000 times that of the deposition gas, deposition of microcrystalline semiconductor and crystal growth are primarily caused by plasma discharge performed later. In the second period, etching of the amorphous semiconductor region is primarily caused.

Radicals are generated from the deposition gas containing silicon or germanium along with hydrogen radicals in plasma in the first period and the second period. When the pressure in the process chamber is set higher than or equal to 1333 Pa and

12

lower than or equal to 50000 Pa (higher than or equal to 10 Torr and lower than or equal to 370 Torr), further preferably higher than or equal to 1333 Pa and lower than or equal to 13332 Pa (higher than or equal to 10 Torr and lower than or equal to 100 Torr), the mean free path of the deposition gas is short because of such high pressure in the process chamber; thus, hydrogen radicals and hydrogen ions lost energy every time they collide with each other. Accordingly, the energy of hydrogen radicals and hydrogen ions when they reach the first microcrystalline semiconductor film 59 becomes lower.

In the first period in which the flow rate of the deposition gas containing silicon or germanium is high (the period with the flow rate c in FIG. 2) under the above-described pressure, the number of radicals generated from the deposition gas containing silicon or germanium is larger than that in the second period with the flow rate b, so that deposition and crystal growth of microcrystalline semiconductor are primarily caused rather than the etching on the surface of the first microcrystalline semiconductor film 59. When the pressure in the process chamber is set to the above-described level, the energy of radicals and ions becomes lower, which leads to reduction of plasma damage on the second microcrystalline semiconductor film 61 during deposition, contributing to reduction of defects.

In the second period in which the flow rate of the deposition gas containing silicon or germanium is low (the period with the flow rate b in FIG. 2) under the above-described pressure, the amorphous semiconductor region included in the first microcrystalline semiconductor film 59 which is formed under the second condition and the microcrystalline semiconductor deposited over the first microcrystalline semiconductor film 59 is selectively etched by hydrogen radicals dissociated in plasma; accordingly, the crystallites are exposed.

By repeating the above-described first period and second period, exposure of the crystallites owing to the primary etching of the amorphous semiconductor region in the second period and the crystal growth in which the exposed crystallites are used as nuclei in the first period are alternately performed. Accordingly, the size of the crystallites in the mixed phase grains is increased, and further the crystal growth is caused to form crystals having an orientation plane. Since the second period is longer than the first period, the amorphous semiconductor region in the microcrystalline semiconductor is sufficiently etched; thus, the amount of amorphous semiconductor included in the second microcrystalline semiconductor film can be reduced. As a result, the second microcrystalline semiconductor film having higher crystallinity than the first microcrystalline semiconductor film can be formed without increasing the space between the mixed phase grains in the first microcrystalline semiconductor film. Further, defects of the second microcrystalline semiconductor film 61 can be reduced.

In the second period, by setting the flow rate of the deposition gas containing silicon or germanium to a slight flow rate, typically to a flow rate of more than 0 sccm and less than or equal to 0.3 sccm, a slight amount of radicals (typically silyl radicals) generated from the deposition gas is bonded to dangling bonds of the crystallites that are exposed by etching of the amorphous semiconductor region; thus, high crystallinity can be obtained through crystal growth. That is, crystal growth occurs concurrently with the etching, whereby the crystallinity of the second microcrystalline semiconductor film 61 is increased.

Note that here, after the first period in which the deposition gas containing silicon or germanium flows with the flow rate c, the second period in which the deposition gas containing silicon or germanium flows with the flow rate b follows;

13

however, after the second period in which the deposition gas containing silicon or germanium flows with the flow rate b , the first period in which the deposition gas containing silicon or germanium flows with the flow rate c may follow. Note that t_1 and h are each preferably several seconds to several tens of seconds. When t_1 and t_2 are each several minutes, for example, a microcrystalline semiconductor film having low crystallinity with a thickness of several nanometers is formed in t_1 , and only a surface of the microcrystalline semiconductor film is reacted in t_2 . Accordingly, it is difficult to increase the crystallinity in the microcrystalline semiconductor film.

Note that here, each of all the first periods, i.e., each of all periods in which the deposition gas containing silicon or germanium flows with the flow rate c , takes t_1 seconds; however, they may take different times. Further, here, each of all the second periods, i.e., each of all periods in which the deposition gas containing silicon or germanium flows with the flow rate b ($b < c$), takes t_2 seconds; however, they may take different times.

Further, as shown by the solid line **79** in FIG. 2, a rare gas such as helium, neon, argon, krypton, or xenon is not introduced into the source gas. However, as shown by a dashed line **77**, such a rare gas may be introduced into the process chamber. Alternatively, a rare gas whose flow rate is alternately increased and decreased may be introduced into the process chamber.

Note that although the flow rate of hydrogen is fixed here, the flow rate of hydrogen may be changed as needed to form the second microcrystalline semiconductor film **61**. Alternatively, the flow rate of the deposition gas containing silicon or germanium may be fixed and the flow rate of hydrogen may be alternately increased and decreased.

By changing the flow rate of the source gas while the high-frequency power supply is kept on, the deposition rate of the second microcrystalline semiconductor film **61** can be improved.

Note that after the deposition gas containing silicon or germanium is introduced into the process chamber with the flow rate c , that is, after the first period, the high-frequency power supply may be turned off. Alternatively, after the deposition gas containing silicon or germanium is introduced into the process chamber with the flow rate b , that is, after the second period, the high-frequency power supply may be turned off.

Here, the flow rate h of the deposition gas containing silicon or germanium has the relation: $0 < b < c$. However, the flow rate b may be 0. That is, the period in which the deposition gas containing silicon or germanium is introduced and the period in which the deposition gas containing silicon or germanium is not introduced may be alternately provided. As shown by a dashed line **72**, the power may be increased in the first period in order to increase the deposition rate, and the power may be decreased in the second period in order to suppress the etching of the crystallites included in the microcrystalline semiconductor.

Note that if the pressure in the process chamber is higher than or equal to 1333 Pa and lower than or equal to 50000 Pa (higher than or equal to 10 Torr and lower than or equal to 370 Torr), preferably higher than or equal to 1333 Pa and lower than or equal to 13332 Pa (higher than or equal to 10 Torr and lower than or equal to 100 Torr), the pressure in the second condition may be higher than that in the first condition, the pressure in the first condition may be higher than that in the second condition, or alternatively, the pressure in the first condition may be equal to that in the second condition.

Through the above-described process, a microcrystalline semiconductor film **62** including the seed crystal **57**, the first

14

microcrystalline semiconductor film **59**, and the second microcrystalline semiconductor film **61** can be formed.

Here, conceptual diagrams illustrating film formation of the microcrystalline semiconductor film **62** described in this embodiment are shown in FIGS. 1D to 1F. FIGS. 1D to 1F are enlarged views schematically showing the deposition state in FIGS. 1A to 1C.

As illustrated in FIG. 1D, the deposition step of the seed crystal **57** is a step for dispersing the mixed phase grains **57a** in order to increase the size of the mixed phase grains included in the microcrystalline semiconductor film **62** formed later. Therefore, in the seed crystal **57**, the mixed phase grains **57a** are deposited with the space **57b** provided therebetween as illustrated in FIG. 1D.

As illustrated in FIG. 1E, the deposition step of the first microcrystalline semiconductor film **59** is a step for causing crystal growth using the mixed phase grains **57a** as nuclei and thereby forming a film including mixed phase grains with extremely little space provided therebetween. Thus, crystal growth is caused using the mixed phase grains **57a** as seeds, so that microcrystalline semiconductors **58** are deposited.

When the pressure in the process chamber is higher than or equal to 1333 Pa and lower than or equal to 50000 Pa (higher than or equal to 10 Torr and lower than or equal to 370 Torr), preferably higher than or equal to 1333 Pa and lower than or equal to 13332 Pa (higher than or equal to 10 Torr and lower than or equal to 100 Torr), the microcrystalline semiconductors **58** grow not only in the film thickness direction but also in the plane direction. As a result, spaces between the microcrystalline semiconductors **58** are filled and the microcrystalline semiconductors **58** become in contact with each other.

As illustrated in FIG. 1F, the deposition step of the second microcrystalline semiconductor film **61** is a step for depositing microcrystalline semiconductors **60** having higher crystallinity over the microcrystalline semiconductors **58**. In the deposition step of the second microcrystalline semiconductor film **61**, the step for deposition and crystal growth of microcrystalline semiconductor and the step for primarily etching an amorphous semiconductor region included in the microcrystalline semiconductor and exposing crystallites included in the microcrystalline semiconductor are performed alternately. Further, since the pressure in the process chamber is higher than or equal to 1333 Pa and lower than or equal to 50000 Pa (higher than or equal to 10 Torr and lower than or equal to 370 Torr), preferably higher than or equal to 1333 Pa and lower than or equal to 13332 Pa (higher than or equal to 10 Torr and lower than or equal to 100 Torr), the amorphous semiconductor region in the microcrystalline semiconductor is primarily etched. For these reasons, epitaxial growth is likely to be caused at the time of deposition of the microcrystalline semiconductor on the exposed crystallites. Accordingly, in the deposition step of the second microcrystalline semiconductor film **61**, orientation of the microcrystalline semiconductor becomes higher and the microcrystalline semiconductors **60** having an orientation plane are deposited.

Through the steps of FIGS. 1D to 1F, the microcrystalline semiconductor film **62** including mixed phase grains, which has high crystallinity, extremely little space between the mixed phase grains, and an orientation plane, can be formed. The mixed phase grains included in the microcrystalline semiconductor film **62** may be the microcrystalline semiconductor deposited in the seed crystal **57**, the first microcrystalline semiconductor film **59**, or the second microcrystalline semiconductor film **61**. Alternatively, the mixed phase grains included in the microcrystalline semiconductor film **62** may be the microcrystalline semiconductor formed by deposition and crystal growth of two or more of the seed crystal **57**, the

15

first microcrystalline semiconductor film 59, and the second microcrystalline semiconductor film 61.

Here, the shape of the microcrystalline semiconductor film 62 will be described with reference to FIG. 3.

FIG. 3 is a schematic cross-sectional view of the microcrystalline semiconductor film 62. The microcrystalline semiconductor film 62 having a thickness of more than or equal to 70 nm and less than or equal to 100 nm includes a mixed phase grain 47 part of which projects from a surface of the microcrystalline semiconductor film 62. Although a plurality of mixed phase grains is mixed in a region 45 where mixed phase grains do not project from the surface, the microcrystalline semiconductor film 62 has such a feature that the mixed phase grain 47 having a larger diameter than the mixed phase grain in the region 45 projects from the surface. Further, the mixed phase grain 47 projecting from the surface has a feature of having an orientation plane in the region where the mixed phase grain projects from the surface. Therefore, the mixed phase grain 47 has an angular region when seen from the above. The angular region has a straight side in a cross-sectional shape. That is, a mixed phase grain having high orientation ratio, that is, having a large crystallite is included on the surface side of the microcrystalline semiconductor film 62. The size of the crystallite at this time is 13 nm or more, further preferably 15 nm or more.

The size of the crystallite is calculated by substituting the width at half the intensity of a peak indicating a plane orientation in the spectrum measured by X-ray diffraction, that is, the full width at half maximum, into Formula 1. Note that the size L of the crystallite obtained according to Formula 1 is the average size of a crystallite having a plane orientation represented by the peak in the microcrystalline semiconductor film.

$$L = K\lambda / (\beta \cos \theta) \quad (\text{Formula 1})$$

Note that K is the Scherrer constant, λ is a wavelength of x-rays, β is a full width at half maximum, and θ is a diffraction angle.

Thus, when the microcrystalline semiconductor film 62 is observed with a transmission electron microscope, the mixed phase grains 47 that have substantially the same contrast are observed on the surface side of the microcrystalline semiconductor film 62. Note that the crystallite in the mixed phase grain 47 may be a twin crystal. Further, the crystallite in the mixed phase grain 47 may include a defect.

The space between adjacent mixed phase grains is extremely little and the mixed phase grains are densely packed in the microcrystalline semiconductor film 62; thus, the film density measured by X-ray reflectometry is higher than or equal to 2.25 g/cm³ and lower than or equal to 2.35 g/cm³, preferably higher than or equal to 2.30 g/cm³ and lower than or equal to 2.33 g/cm³. The film density of single crystal silicon is 2.33 g/cm³; thus, the microcrystalline semiconductor film formed in this embodiment can be said to have a high density and little space. Note that the measured film density may be higher than the film density of single crystal silicon due to measurement variation.

The thickness of the seed crystal 57 is preferably more than or equal to 1 nm and less than or equal to 10 nm. If the thickness of the seed crystal 57 is more than 10 nm, even when the first microcrystalline semiconductor film 59 is deposited, it is difficult to fill the space between the mixed phase grains 57a and to etch the amorphous semiconductor included in the seed crystal 57, which leads to reduction in the crystallinity of the seed crystal 57 and the first microcrystalline semiconductor film 59. In addition, since the mixed phase grain needs to

16

be formed in the seed crystal 57, the thickness of the seed crystal 57 is preferably more than or equal to 1 nm.

The total thickness of the first microcrystalline semiconductor film 59 and the second microcrystalline semiconductor film 61 is preferably more than or equal to 60 nm and less than or equal to 100 nm. When the total thickness of the first microcrystalline semiconductor film 59 and the second microcrystalline semiconductor film 61 is 60 nm or more, variation in electrical characteristics of thin film transistors can be reduced; and when the total thickness of the first microcrystalline semiconductor film 59 and the second microcrystalline semiconductor film 61 is 100 nm or less, throughput can be increased and film peeling due to stress can be suppressed.

The seed crystal 57, the first microcrystalline semiconductor film 59, and the second microcrystalline semiconductor film 61 include a microcrystalline semiconductor. Note that a microcrystalline semiconductor is a semiconductor having an intermediate structure between an amorphous structure and a crystalline structure (including a single crystal structure and a polycrystalline structure). Thus, the microcrystalline semiconductor includes an amorphous semiconductor region. A microcrystalline semiconductor is a semiconductor having a third state that is stable in terms of free energy and is a crystalline semiconductor having short-range order and lattice distortion, in which columnar or needle-like mixed phase grains having a diameter greater than or equal to 2 nm and less than or equal to 200 nm, preferably greater than or equal to 10 nm and less than or equal to 80 nm, further preferably greater than or equal to 20 nm and less than or equal to 50 nm grow in a direction normal to the substrate surface. Therefore, there is a case in which a crystal grain boundary is formed at the interface between the columnar or needle-like mixed phase grains. Note that the diameter of a crystal grain means the maximum diameter of a crystal grain in a plane parallel to the substrate surface.

The peak of the Raman spectrum of microcrystalline silicon, which is a typical example of a microcrystalline semiconductor, is located in a lower wave number side than 520 cm⁻¹ which represents single crystal silicon. That is, the peak of the Raman spectrum of the microcrystalline silicon exists between 520 cm⁻¹ which represents single crystal silicon and 480 cm⁻¹ which represents amorphous silicon. In addition, microcrystalline silicon includes hydrogen or halogen at 1 atomic % or more in order to terminate dangling bonds. Moreover, microcrystalline semiconductor has increased stability and is preferable when containing a rare gas element such as helium, neon, argon, krypton, or xenon to further enhance lattice distortion. Such a description of the microcrystalline semiconductor is disclosed in, for example, U.S. Pat. No. 4,409,134.

According to this embodiment, a microcrystalline semiconductor film whose crystallinity is increased by reduction of a space between mixed phase grains can be formed. (Embodiment 2)

In this embodiment, a method for manufacturing a thin film transistor formed in a semiconductor device that is one embodiment of the present invention will be described with reference to FIGS. 4A to 4E, FIGS. 5A and 513, FIGS. 6A to 6C, and FIGS. 7A to 7D. Note that an n-channel thin film transistor has higher carrier mobility than a p-channel thin film transistor. Further, it is preferable that all thin film transistors formed over the same substrate have the same polarity because the number of manufacturing steps can be reduced in such a case. In this embodiment, a method for manufacturing an n-channel thin film transistor will be described.

17

Note that the term “on-state current” refers to current which flows between a source electrode and a drain electrode when a thin film transistor is on. For example, in the case of an n-channel thin film transistor, the on-state current refers to current which flows between a source electrode and a drain electrode when gate voltage is higher than the threshold voltage of the transistor.

In addition, the term “off-state current” refers to current which flows between a source electrode and a drain electrode when a thin film transistor is off. For example, in the case of an n-channel thin film transistor, the off-state current refers to current which flows between a source electrode and a drain electrode when gate voltage is lower than the threshold voltage of the thin film transistor.

As illustrated in FIG. 4A, a gate electrode **103** is formed over a substrate **101**. Then, a gate insulating film **105** which covers the gate electrode **103** (also referred to as a first gate electrode) is formed. A seed crystal **107** is formed over the gate insulating film **105**.

As the substrate **101**, any of the substrates that can be used as the substrate **51** described in Embodiment 1 can be used as appropriate.

The gate electrode **103** can be formed as a single layer or a stacked layer using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, scandium, or nickel or an alloy material which includes any of these material materials as a main component. Further, a semiconductor typified by polycrystalline silicon doped with an impurity element such as phosphorus, an Ag—Pd—Cu alloy, an Al—Nd alloy, an Al—Ni alloy, or the like may be used.

The following are preferable examples of the two-layer structure of the gate electrode **103**: a two-layer structure in which a molybdenum film is provided over an aluminum film, a two-layer structure in which a molybdenum film is provided over a copper film, a two-layer structure in which a titanium nitride film or a tantalum nitride film is provided over a copper film, a two-layer structure in which a titanium nitride film and a molybdenum film are stacked, a two-layer structure in which a film of a copper-magnesium alloy containing oxygen and a copper film are stacked, a two-layer structure in which a film of a copper-manganese alloy containing oxygen and a copper film are stacked, a two-layer structure in which a copper-manganese alloy film and a copper film are stacked, or the like. As a three-layer structure, it is preferable to stack a tungsten film or a tungsten nitride film, an alloy film of aluminum and silicon or an alloy film of aluminum and titanium, and a titanium nitride film or a titanium film. By stacking a metal film serving as a barrier film over a film having low electric resistance, electric resistance of the gate electrode **103** can be low and diffusion of metal elements from the metal thin into the semiconductor film can be prevented.

The gate electrode **103** can be formed in the following manner: a conductive film is formed over the substrate **101** by a sputtering method or a vacuum evaporation method using any of the above materials; a mask is formed over the conductive film by a photolithography method, an inkjet method, or the like; and the conductive film is etched using the mask. Alternatively, the gate electrode **103** can be formed by discharging a conductive nanopaste of silver, gold, copper, or the like over the substrate by an inkjet method and baking the conductive nanopaste. In order to improve adhesion between the gate electrode **103** and the substrate **101**, a nitride film of any of the above metal materials may be provided between the substrate **101** and the gate electrode **103**. In this embodiment, a conductive film is formed over the substrate **101** and etched using a resist mask formed by a photolithography method.

18

Note that a side surface of the gate electrode **103** preferably has a tapered shape in order to prevent an insulating film, a semiconductor film, and a wiring formed over the gate electrode **103** in later steps from being cut at a step portion of the gate electrode **103**. To form the gate electrode **103** having a tapered shape, etching may be performed while the resist mask is made to recede.

In the step of forming the gate electrode **103**, a gate wiring (a scan line) and a capacitor wiring can also be formed at the same time. The scan line refers to a wiring for selecting a pixel, and the capacitor wiring refers to a wiring which is connected to one of electrodes of a storage capacitor in a pixel. However, without limitation thereto, the gate electrode **103** and one of or both the gate wiring and the capacitor wiring may be formed separately.

The gate insulating film **105** (also referred to as a first gate insulating film) can be formed using any of the insulating films that can be used as the insulating film **55** described in Embodiment 1 as appropriate. By forming the gate insulating film **105** using an oxide insulating film such as a silicon oxide film or a silicon oxynitride film, fluctuation in threshold voltage of the thin film transistor can be reduced.

The gate insulating film **105** can be formed by a CVD method, a sputtering method, or the like. The condition for the deposition of the seed crystal **57** which is described in Embodiment 1 can be employed as appropriate to generate the glow discharge plasma in the step of forming the gate insulating film **105** by a CVD method. When the gate insulating film **105** is formed at a high frequency of 1 GHz or more with a microwave plasma CVD apparatus, the breakdown voltage between the gate electrode and the drain and source electrodes can be improved, whereby a highly reliable thin film transistor can be obtained.

Further, by forming a silicon oxide film by a CVD method using an organosilane gas as the gate insulating film **105**, the crystallinity of the semiconductor film which is formed later can be increased, whereby the on-state current and the field-effect mobility of the thin film transistor can be increased. Examples of the organosilane gas include silicon-containing compounds such as tetraethoxysilane (TEOS) (chemical formula: $\text{Si}(\text{OC}_2\text{H}_5)_4$), tetramethylsilane (TMS) (chemical formula: $\text{Si}(\text{CH}_3)_4$), tetramethylcyclotetrasiloxane (TMCTS), octamethylcyclotetrasiloxane (OMCTS), hexamethyldisilazane (HMDS), triethoxysilane ($\text{SiH}(\text{OC}_2\text{H}_5)_3$), and trisdimethylaminosilane ($\text{SiH}(\text{N}(\text{CH}_3)_2)_3$).

The seed crystal **107** can be formed under the first condition that enables the mixed phase grains having high crystallinity to be formed at a low density, in a manner similar to that of the seed crystal **57** described in Embodiment 1.

In the case where a rare gas such as helium, neon, argon, krypton, or xenon is added to the source gas of the seed crystal **107**, the crystallinity of the seed crystal **107** can be increased. Accordingly, the on-state current and the field-effect mobility of the thin film transistor can be increased.

Then, as illustrated in FIG. 4B, a first microcrystalline semiconductor film **109** is formed over the seed crystal **107**. In a manner similar to that of the first microcrystalline semiconductor film **59** described in Embodiment 1, the first microcrystalline semiconductor film **109** can be formed under the second condition that enables the crystallites in the seed crystal **107** to grow to fill a space between the mixed phase grains.

In the case where a rare gas such as helium, neon, argon, krypton, or xenon is added to the source gas of the first microcrystalline semiconductor film **109**, the crystallinity of the first microcrystalline semiconductor film **109** can be improved as in the case of the seed crystal **107**. Accordingly,

the on-state current and the field-effect mobility of the thin film transistor can be increased.

Next, as illustrated in FIG. 4C, a second microcrystalline semiconductor film **110** is formed over the first microcrystalline semiconductor film **109**. The second microcrystalline semiconductor film **110** can be formed under the third condition that allows a microcrystalline semiconductor film having high crystallinity to be formed without increasing the space between the mixed phase grains included in the first microcrystalline semiconductor film **109**, in a manner similar to that of the second microcrystalline semiconductor film **61** described in Embodiment 1.

Then, as illustrated in FIG. 4D, a semiconductor film **111** is formed over the second microcrystalline semiconductor film **110**. The semiconductor film **111** includes a microcrystalline semiconductor region **111a** and an amorphous semiconductor region **111b**. Then, an impurity semiconductor film **113** is formed over the semiconductor film **111**. Then, a mask **115** is formed of a resist over the impurity semiconductor film **113**.

The semiconductor film **111** including the microcrystalline semiconductor region **111a** and the amorphous semiconductor region **111b** can be formed under a condition which causes partial crystal growth using the second microcrystalline semiconductor film **110** as a nucleus (a condition under which the crystal growth is suppressed).

The semiconductor film **111** is formed in a process chamber of a plasma CVD apparatus by glow discharge plasma using a mixture of a deposition gas containing silicon or germanium, hydrogen, and a gas containing nitrogen. Examples of the gas containing nitrogen include ammonia, nitrogen, nitrogen fluoride, nitrogen chloride, chloroamine, fluoroamine, and the like. Glow discharge plasma can be generated as in the case of the seed crystal **107**.

In this case, the flow rate ratio of hydrogen to the deposition gas containing silicon or germanium is set to a flow rate ratio with which a microcrystalline semiconductor film is formed as in the case of forming the seed crystal **107**, the first microcrystalline semiconductor film **109**, or the second microcrystalline semiconductor film **110**, and a gas containing nitrogen is used as a source gas, whereby crystal growth can be suppressed as compared to the deposition conditions for the seed crystal **107**, the first microcrystalline semiconductor film **109**, and the second microcrystalline semiconductor film **110**. Specifically, since a gas containing nitrogen is included in the source gas, the crystal growth is partly suppressed at an early stage of the deposition of the semiconductor film **111**; thus, a conical or pyramidal microcrystalline semiconductor region grows, and an amorphous semiconductor region is formed. Furthermore, at a middle stage or later stage of the deposition, the crystal growth of the conical or pyramidal microcrystalline semiconductor region stops, and only an amorphous semiconductor region is deposited. As a result, in the semiconductor film **111**, the microcrystalline semiconductor region **111a** and the amorphous semiconductor region **111b** which is formed using a well-ordered semiconductor film having fewer defects and a steep tail of a level at a band edge in the valence band, can be formed.

Here, a typical example of a condition for forming the semiconductor film **111** is a condition in which the flow rate of hydrogen is 10 times to 2000 times, preferably 10 times to 200 times that of the deposition gas containing silicon or germanium. Note that in a typical example of a condition for forming a normal amorphous semiconductor film, the flow rate of hydrogen is 0 times to 5 times that of the deposition gas containing silicon or germanium.

By adding a rare gas such as helium, neon, argon, krypton, or xenon into a source gas of the semiconductor film **111**, the deposition rate can be increased.

The thickness of the semiconductor film **111** is preferably 50 nm to 350 nm, further preferably 120 nm to 250 nm.

FIGS. 5A and 5B are enlarged views of a portion between the gate insulating film **105** and the impurity semiconductor film **113** illustrated in FIG. 4D.

As illustrated in FIG. 5A, the microcrystalline semiconductor region **111a** in the semiconductor film **111** has a projection and a depression; the projection has a conical or pyramidal shape whose width decreases from the gate insulating film **105** side toward the amorphous semiconductor region **111b** side (a tip of the projection has an acute angle). Note that the microcrystalline semiconductor region **111a** may have a projection whose width increases from the gate insulating film **105** side toward the amorphous semiconductor region **111b** side (an inverted conical or pyramidal shape).

By setting the thickness of the seed crystal **107**, the first microcrystalline semiconductor film **109**, the second microcrystalline semiconductor film **110**, and the microcrystalline semiconductor region **111a**, that is, the distance from the interface between the gate insulating film **105** and the seed crystal **107** to the tip of the projection of the microcrystalline semiconductor region **111a** to greater than or equal to 5 nm and less than or equal to 310 nm, the projection of the microcrystalline semiconductor region **111a** is not in contact with an impurity semiconductor film that is formed later; accordingly, the off-state current of the thin film transistor can be reduced.

Further, it is preferable that the oxygen concentration in the semiconductor film **111** which is measured by secondary ion mass spectrometry (SIMS) be less than 1×10^{18} atoms/cm³, because such an oxygen concentration can increase the crystallinity of the microcrystalline semiconductor region **111a**. The nitrogen concentration profile of the semiconductor film **111** which is measured by secondary ion mass spectrometry has a peak concentration greater than or equal to 1×10^{20} atoms/cm³ and less than or equal to 1×10^{21} atoms/cm³, preferably greater than or equal to 2×10^{20} atoms/cm³ and less than or equal to 1×10^{21} atoms/cm³.

The amorphous semiconductor region **111b** includes an amorphous semiconductor containing nitrogen. Nitrogen in the amorphous semiconductor containing nitrogen may exist, for example, as an NH group or an NH₂ group. Amorphous silicon is used as an amorphous semiconductor.

The amorphous semiconductor containing nitrogen is a semiconductor having lower energy at an Urbach edge measured by a constant photocurrent method (CPM) or photoluminescence spectroscopy and a smaller amount of absorption spectra of defective levels as compared to a conventional amorphous semiconductor. In other words, as compared to the conventional amorphous semiconductor, the amorphous silicon containing nitrogen is a well-ordered semiconductor having fewer defects and a steep tail of a level at a band edge in the valence band. Since the amorphous semiconductor containing nitrogen has a steep tail of a level at a band edge in the valence band, the band gap is wide and tunnel current does not flow easily. Therefore, when the amorphous semiconductor containing nitrogen is provided between the microcrystalline semiconductor region **111a** and the impurity semiconductor film **113**, the off-state current of the thin film transistor can be reduced. In addition, by providing the amorphous semiconductor containing nitrogen, the on-state current and the field-effect mobility can be increased.

Further, a peak of a spectrum of the amorphous semiconductor containing nitrogen obtained by low-temperature pho-

21

photoluminescence spectroscopy is greater than or equal to 1.31 eV and less than or equal to 1.39 eV. Note that a peak region of a spectrum of a microcrystalline semiconductor, typically microcrystalline silicon, obtained by low-temperature photoluminescence spectroscopy is greater than or equal to 0.98 eV and less than or equal to 1.02 eV, which shows that an amorphous semiconductor containing nitrogen is different from a microcrystalline semiconductor.

The microcrystalline semiconductor region 111a, as well as the amorphous semiconductor region 111b, may include a NH group or an NH₂ group.

Further, as illustrated in FIG. 5B, a semiconductor mixed phase grain 111c whose grain size is greater than or equal to 1 nm and less than or equal to 10 nm, preferably greater than or equal to 1 nm and less than or equal to 5 nm is included in the amorphous semiconductor region 111b, whereby the on-state current and the field-effect mobility can be further increased.

A microcrystalline semiconductor having a projection shape (a conical or pyramidal shape) whose width decreases from the gate insulating film 105 side toward the amorphous semiconductor region 111b side is formed in the following manner. After a microcrystalline semiconductor film is formed under a condition where a microcrystalline semiconductor is deposited, crystal growth is caused under a condition where crystal growth is partly caused while an amorphous semiconductor is deposited.

Since the microcrystalline semiconductor region 111a in the semiconductor film 111 has the conical or pyramidal shape or the inverted conical or pyramidal shape, resistance in the vertical direction (in the film thickness direction) of when voltage is applied between the source and drain electrodes in an on state, i.e. the resistance of the semiconductor film 111 can be lowered. Further, tunnel current does not easily flow since the amorphous semiconductor containing nitrogen which is a well-ordered semiconductor having fewer defects and a steep tail of a level at a band edge in the valence band is provided between the microcrystalline semiconductor region 111a and the impurity semiconductor film 113. Thus, in the thin film transistor described in this embodiment, the on-state current and the field-effect mobility can be increased and the off-state current can be reduced.

Here, the semiconductor film 111 including the microcrystalline semiconductor region 111a and the amorphous semiconductor region 111b is formed using the source gas including the gas containing nitrogen. Alternatively, the semiconductor film 111 including the microcrystalline semiconductor region 111a and the amorphous semiconductor region 111b can be formed in the following manner: the top surface of the microcrystalline semiconductor film 109 is exposed to a gas containing nitrogen so that nitrogen is adsorbed to the top surface of the microcrystalline semiconductor film 109, and then film deposition of the semiconductor film 111 including the microcrystalline semiconductor region 111a and the amorphous semiconductor region 111b is performed using hydrogen and a deposition gas containing silicon or germanium as a source gas.

The impurity semiconductor film 113 is formed using amorphous silicon to which phosphorus is added, microcrystalline silicon to which phosphorus is added, or the like. Alternatively, the impurity semiconductor film 113 can have a stacked structure of amorphous silicon to which phosphorus is added and microcrystalline silicon to which phosphorus is added. Note that, in the case of forming a p-channel thin film transistor as a thin film transistor, the impurity semiconductor film 113 is formed using microcrystalline silicon to which boron is added, amorphous silicon to which boron is added, or

22

the like. In the case where the semiconductor film 111 forms an ohmic contact with wirings 129a and 129b which are formed later, the impurity semiconductor film 113 is not necessarily formed.

The impurity semiconductor film 113 is formed in a process chamber of the plasma CVD apparatus by glow discharge plasma using a mixture of hydrogen, phosphine (diluted with hydrogen or silane), and a deposition gas containing silicon, whereby amorphous silicon to which phosphorus is added or microcrystalline silicon to which phosphorus is added is formed. In the ease of manufacturing a p-channel thin film transistor, the impurity semiconductor film 113 may be formed using glow discharge plasma using diborane instead of phosphine.

Further, in the case where the impurity semiconductor film 113 is formed using microcrystalline silicon to which phosphorus is added or microcrystalline silicon to which boron is added, a microcrystalline semiconductor film, typically a microcrystalline silicon film, is formed between the semiconductor film 111 and the impurity semiconductor film 113, so that characteristics of the interface can be improved. As a result, resistance generated at the interface between the impurity semiconductor film 113 and the semiconductor film 111 can be reduced. Therefore, the amount of current flowing through the source region, the semiconductor film, and the drain region of the thin film transistor can be increased and the on-state current and the field-effect mobility can be increased.

The mask 115 formed of a resist can be formed by a photolithography step.

Next, the seed crystal 107, the first microcrystalline semiconductor film 109, the second microcrystalline semiconductor film 110, the semiconductor film 111, and the impurity semiconductor film 113 are selectively etched using the mask 115 formed of the resist. Through this step, the seed crystal 107, the first microcrystalline semiconductor film 109, the second microcrystalline semiconductor film 110, the semiconductor film 111, and the impurity semiconductor film 113 are divided for each element, whereby an island-shaped semiconductor stacked body 117 and an island-shaped impurity semiconductor film 121 are formed. The semiconductor stacked body 117 includes a microcrystalline semiconductor region 117a which includes part of the seed crystal 107, part of the first microcrystalline semiconductor film 109, part of the second microcrystalline semiconductor film 110, and part of the microcrystalline semiconductor region 111a of the semiconductor film 111; and an amorphous semiconductor region 117b which includes part of the amorphous semiconductor region 111b of the semiconductor film 111. Then, the mask 115 formed of the resist is removed (see FIG. 4E).

Next, a conductive film 127 is formed over the impurity semiconductor film 121 (see FIG. 6A). The conductive film 127 can be formed as a single layer or a stacked layer using any of aluminum, copper, titanium, neodymium, scandium, molybdenum, chromium, tantalum, tungsten, and the like. An aluminum alloy to which an element for preventing a hillock is added (e.g., an Al—Nd alloy which can be used for the gate electrode 103) may also be used. Crystalline silicon to which an impurity element which serves as a donor is added may be used. A stacked-layer structure in which a film on the side that is in contact with the crystalline silicon to which an impurity element serving as a donor is added is formed using titanium, tantalum, molybdenum, tungsten, or a nitride of any of these elements, and a layer of aluminum or an aluminum alloy is formed thereover may also be formed. The conductive film 127 may also have a stacked-layer structure where aluminum or an aluminum alloy is provided and titanium, tantalum, molybdenum, tungsten, or nitride of any of these elements is

23

provided thereon and thereunder. The conductive film 127 is formed by a CVD method, a sputtering method, or a vacuum evaporation method. Alternatively, the conductive film 127 may be formed by discharging a conductive nanopaste of silver, gold, copper, or the like by a screen printing method, an inkjet method, or the like and baking the conductive nanopaste.

Then, a mask is formed of a resist by a photolithography step, and the conductive film 127 is etched with the use of the resist mask, whereby the wirings 129a and 129b serving as a source electrode and a drain electrode are formed (see FIG. 6B).

The etching of the conductive film 127 may be either dry etching or wet etching. Note that one of the wirings 129a and 129b serves as a signal line as well as a source electrode or a drain electrode. However, without limitation thereto, a signal line may be provided separately from the source and drain electrodes.

Then, the impurity semiconductor film 121 and the semiconductor stacked body 117 are partly etched, whereby a pair of impurity semiconductor films 131a and 131b serving as a source and drain regions is formed. Also, a semiconductor stacked body 133 including a microcrystalline semiconductor region 133a and a pair of amorphous semiconductor regions 133b is formed. At this point, the semiconductor stacked body 117 is etched so that the microcrystalline semiconductor region 133a is exposed, whereby the semiconductor stacked body 133 having the following structure is formed: in regions which are covered with the wirings 129a and 129b, the microcrystalline semiconductor region 133a and the amorphous semiconductor regions 133b are stacked, and in a region which is covered with neither the wiring 129a nor the wiring 129b and overlaps with at least the gate electrode, the microcrystalline semiconductor region 133a is exposed.

Here, ends of the wirings 129a and 129b are aligned with ends of the impurity semiconductor films 131a and 131b. However, the ends of the wirings 129a and 129b and the ends of the impurity semiconductor films 131a and 131b are not necessarily aligned with each other; the ends of the wirings 129a and 129b may be positioned on the inner side than the ends of the impurity semiconductor films 131a and 131b in a cross section.

Next, dry etching may be performed. The dry etching is performed under a condition where the exposed microcrystalline semiconductor region 133a and the exposed amorphous semiconductor regions 133b are not damaged and the etching rates of the microcrystalline semiconductor region 133a and the amorphous semiconductor regions 133b are low. As an etching gas, Cl₂, CF₄, N₂, or the like is typically used. There is no particular limitation on an etching method, and an inductively coupled plasma (ICP) method, a capacitively coupled plasma (CCP) method, an electron cyclotron resonance (ECR) method, a reactive ion etching (RIE) method, or the like can be used.

Then, the surfaces of the microcrystalline semiconductor region 133a and the amorphous semiconductor regions 133b are subjected to plasma treatment typified by water plasma treatment, oxygen plasma treatment, ammonia plasma treatment, nitrogen plasma treatment, plasma treatment using a mixed gas of oxygen and hydrogen, or the like.

After that, the mask formed of a resist is removed. The mask formed of a resist may be removed before the dry etching of the impurity semiconductor film 121 and the semiconductor stacked body 117.

As described above, after the microcrystalline semiconductor region 133a and the amorphous semiconductor regions 133b are formed, dry etching is additionally per-

24

formed under a condition where the microcrystalline semiconductor region 133a and the amorphous semiconductor regions 133b are not damaged, whereby an impurity such as a residue over the exposed microcrystalline semiconductor region 133a and the exposed amorphous semiconductor regions 133b can be removed. Further, after the dry etching, water plasma treatment or plasma treatment using a mixed gas of oxygen and hydrogen is successively performed, whereby a residue of the resist mask can be removed and defects of the microcrystalline semiconductor region 133a can be reduced. Further, by the plasma treatment, a higher insulating property between the source region and the drain region can be obtained. Thus, in the resulting thin film transistors, off-state current can be reduced and a variation in electrical characteristics can be reduced.

Note that the mask is formed of a resist by a photolithography step over the conductive film 127, and the conductive film 127 is etched using the resist mask; whereby the wirings 129a and 129b serving as the source and drain electrodes are formed. Then, the impurity semiconductor film 121 is etched, whereby the pair of impurity semiconductor films 131a and 131b serving as the source and drain regions is formed. At this time, part of the semiconductor stacked body 117 is etched in some cases. Then, the semiconductor stacked body 117 may be partly etched after the mask formed of a resist is removed to form the semiconductor stacked body 133 including the microcrystalline semiconductor region 133a and the pair of amorphous semiconductor regions 133b.

Since the microcrystalline semiconductor region 117a is covered with the amorphous semiconductor region 117b in the step of removing the mask formed of a resist, the microcrystalline semiconductor region 117a is prevented from being in contact with a resist stripper and a residue of the resist. Further, since the amorphous semiconductor region 117b is etched using the wirings 129a and 129b to expose the microcrystalline semiconductor region 133a after the mask formed of a resist is removed, the amorphous semiconductor region which is in contact with the resist stripper and a residue of the resist is not left in a back channel. Consequently, leakage current due to the resist stripper and the residue of the resist left in the back channel is not generated, which can further reduce the off state current of the thin film transistor.

Through the above-described process, a single-gate thin film transistor can be manufactured. With the structure described in this embodiment; a single-gate thin film transistor with low off-state current, high on-state current, and high field-effect mobility can be manufactured with high productivity.

Then, an insulating film (also referred to as a second gate insulating film) 137 is formed over the semiconductor stacked body 133, the impurity semiconductor films 131a and 131b, and the wirings 129a and 129b. The insulating film 137 can be formed in a manner similar to that of the gate insulating film 105.

Then, an opening (not illustrated) is formed in the insulating film 137 with the use of a mask which is formed of a resist by a photolithography step. Then, a back gate electrode (also referred to as a second gate electrode) 139 is formed over the insulating film 137 (see FIG. 6C). Through the above-described process, a dual-gate thin film transistor can be manufactured. Although not shown, a pixel electrode connected to one of the wirings 129a and 129b can be formed at the same time as the formation of the back gate electrode 139.

The back gate electrode 139 can be formed in a manner similar to that of the wirings 129a and 129b. The back gate electrode 139 can be formed using a light-transmitting conductive material such as indium oxide containing tungsten

25

oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium tin oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added.

Alternatively, the back gate electrode **139** can be formed using a conductive composition including a conductive high molecule (also referred to as a conductive polymer) having a light-transmitting property. The back gate electrode **139** preferably has a sheet resistance of 10000 Ω /sq. or less and a light transmittance of 70% or greater at a wavelength of 550 nm. Further, the resistivity of the conductive high molecule included in the conductive composition is preferably 0.1 Ω -cm or less.

As the conductive high molecule, a so-called π -electron conjugated conductive high molecule can be used. For example, polyaniline and a derivative thereof, polypyrrole and a derivative thereof, polythiophene and a derivative thereof, and a copolymer of two or more of aniline, pyrrole, and thiophene and a derivative thereof can be given.

The back gate electrode **139** can be formed by forming a thin film using any of the above materials by a CVD method, a sputtering method, or a vacuum evaporation method, and then etching the thin film using a mask formed of a resist by a photolithography step. Alternatively, the back gate electrode **139** can be formed by discharging a conductive nanopaste of silver, gold, copper, or the like by a screen printing method, an inkjet method, or the like and baking the conductive nanopaste.

Next, the shape of the back gate electrode is described with reference to FIGS. 7A to 7D, which are plan views of the thin film transistor.

As illustrated in FIG. 7A, the back gate electrode **139** can be formed in parallel to the gate electrode **103**. In this case, potential applied to the back gate electrode **139** and potential applied to the gate electrode **103** can be controlled independently. Thus, the threshold voltage of the thin film transistor can be controlled. Further, regions in which carriers flow, that is, channel regions are formed on the gate insulating film **105** side and on the insulating film **137** side in the microcrystalline semiconductor region; thus, the on-state current of the thin film transistor can be increased.

As illustrated in FIG. 7B, the back gate electrode **139** can be connected to the gate electrode **103**. That is, the gate electrode **103** and the back gate electrode **139** can be connected through an opening **150** formed in the gate insulating film **105** and the insulating film **137**. In this case, potential applied to the back gate electrode **139** and potential applied to the gate electrode **103** are equal. Therefore, regions in which carriers flow in a semiconductor film, that is, channel regions are formed on the gate insulating film **105** side and on the insulating film **137** side in the microcrystalline semiconductor region; thus, the on-state current of the thin film transistor can be increased.

Further alternatively, as illustrated in FIG. 7C, a structure in which the back gate electrode **139** is not connected to the gate electrode **103** and is in a floating state can be employed. In that case, channel regions are formed on the gate insulating film **105** side and on the insulating film **137** side in the microcrystalline semiconductor region without potential applied to the back gate electrode **139**; thus, the on-state current of the thin film transistor can be increased.

Further, as illustrated in FIG. 7D, the back gate electrode **139** may overlap with the wirings **129a** and **129b** with the insulating film **137** provided therebetween. Although the back gate electrode **139** of FIG. 7A is used in FIG. 7D, it is possible that the back gate electrode **139** of FIG. 7B or FIG. 7C overlap with the wirings **129a** and **129b**.

26

In each of the single-gate thin film transistor and the dual-gate thin film transistor which are described in this embodiment, a channel region can be formed using a microcrystalline semiconductor film whose crystallinity is increased by reduction of a space between mixed phase grains. Therefore, the number of carriers that move in the single-gate thin film transistor and dual-gate thin film transistor is increased, so that the on-state current and the field-effect mobility can be increased. Further, since the microcrystalline semiconductor film having high crystallinity not only on the first gate insulating film side but also on the second gate insulating film side is used as the channel region, the number of carriers that move in the dual-gate thin film transistor is increased, so that the on-state current and the field-effect mobility can be increased. Furthermore, since the amorphous semiconductor regions **133b** are provided between the microcrystalline semiconductor region **133a** and the impurity semiconductor films **131a** and **131b**, the off-state current of the thin film transistor can be reduced. Accordingly, the area of the single-gate thin film transistor and the area of the dual-gate thin film transistor can be reduced, which enables high integration of a semiconductor device. Further, when the thin film transistor described in this embodiment is used for a driver circuit of a display device, the area of the driver circuit can be decreased, which enables the frame of the display device to be narrowed. (Embodiment 3)

In this embodiment, a method for manufacturing a thin film transistor, by which the off-state current can be further reduced as compared to the off-state current in Embodiment 2, will be described with reference to FIGS. 4A to 4C and FIGS. 8A to 8C.

As in Embodiment 2, the semiconductor stacked body **117** in FIG. 8A is formed through the process illustrated in FIGS. 4A to 4C.

Next, plasma treatment is performed in which a side surface of the semiconductor stacked body **117** is exposed to plasma **123** with the mask **115** formed of a resist left. Here, plasma is generated in an oxidizing gas atmosphere or a nitriding gas atmosphere, and the semiconductor stacked body **117** is exposed to the plasma **123**. Examples of the oxidizing gas include oxygen, ozone, dinitrogen monoxide, water vapor, and a mixed gas of oxygen and hydrogen. Examples of the nitriding gas include nitrogen, ammonia, nitrogen fluoride, nitrogen chloride, chloroamine, and fluoroamine. By generating plasma in an oxidizing gas or a nitriding gas, a radical is generated. The radical reacts with the semiconductor stacked body **117**, so that an insulating region that is an oxide or nitride is formed on the side surface of the semiconductor stacked body **117**. Note that instead of irradiation with plasma, irradiation with ultraviolet light may be performed for generation of a radical.

In the case of using oxygen, ozone, water vapor, or a mixed gas of oxygen and hydrogen as the oxidizing gas, the resist recedes by plasma irradiation, whereby a mask **115a** having a smaller bottom surface is formed as illustrated in FIG. 8B. Consequently, through the plasma treatment, the exposed impurity semiconductor film **121** is oxidized in addition to the side surface of the semiconductor stacked body **117**, whereby an insulating region **125** that is an oxide or nitride is formed on the side surface of the semiconductor stacked body **117** and on the side surface and part of the top surface of the impurity semiconductor film **121**.

Next, as described in Embodiment 2, through the process illustrated in FIGS. 6A and 6B, the wirings **129a** and **129b** serving as a source electrode and a drain electrode, the pair of impurity semiconductor films **131a** and **131b** serving as a source region and a drain region, the semiconductor stacked

body 133 including the microcrystalline semiconductor region 133a and the pair of amorphous semiconductor regions 133b, and the insulating film 137 are formed as illustrated in FIG. 8C. Thus, a single-gate thin film transistor can be manufactured.

When a back gate electrode is formed over the insulating film 137, a dual-gate thin film transistor can be manufactured.

In the single-gate thin film transistor and the dual-gate thin film transistor which are described in this embodiment, the channel region can be formed using a microcrystalline semiconductor film whose crystallinity is increased by reduction of a space between mixed phase grains. Furthermore, by providing the insulating region, which is an oxide or nitride, between the semiconductor stacked body 133 and the wiring 129a or 129b, holes injected from the wiring 129a or 129b to the semiconductor stacked body 133 can be reduced; thus, the off-state current of the thin film transistor is reduced and the on-state current and the field-effect mobility of the thin film transistor are increased. Accordingly, the area of the thin film transistor can be reduced, which enables high integration of a semiconductor device. Further, when the thin film transistor described in this embodiment is used for a driver circuit of a display device, the size of the driver circuit can be decreased, which enables the frame of the display device to be narrowed.

In this embodiment, the description is made with reference to Embodiment 2, however, the description can be made with reference to another embodiment as appropriate. (Embodiment 4)

In this embodiment, a method for manufacturing a thin film transistor formed in a semiconductor device that is one embodiment of the present invention will be described with reference to FIGS. 4A to 4D, FIGS. 6A to 6C, and FIG. 9. FIG. 9 shows a step corresponding to the step illustrated in FIG. 6B.

As in Embodiment 2, the conductive film 127 is formed through the process of FIGS. 4A to 4D and FIG. 6A.

Then, as illustrated in FIG. 9, the wirings 129a and 129b are formed and the impurity semiconductor film 121 and the semiconductor stacked body 117 are partly etched, whereby the pair of impurity semiconductor films 131a and 131b serving as a source and drain regions is formed as in Embodiment 2. Also, a semiconductor stacked body 143 including a microcrystalline semiconductor region 143a and an amorphous semiconductor region 143b is formed. At this point, part of the impurity semiconductor film and part of the amorphous semiconductor region are etched, whereby the semiconductor stacked body 143 having the following structure is formed: in the regions which are covered with the wirings 129a and 129b, the microcrystalline semiconductor region 143a and the amorphous semiconductor region 143b are stacked, and in the region which is covered with neither the wiring 129a nor the wiring 129b and overlaps with the gate electrode, the microcrystalline semiconductor region 143a is not exposed and the amorphous semiconductor region 143b is exposed. Note that the etching amount of the semiconductor stacked body 117 here is smaller than that in the case illustrated in FIG. 6B.

The subsequent steps are similar to those in Embodiment 2.

Through the above-described process, a single-gate thin film transistor can be manufactured. Since the back channel side is amorphous in this thin film transistor, the off-state current can be reduced as compared to the thin film transistor illustrated in FIG. 6B.

In this embodiment, after the step illustrated in FIG. 9, the back gate electrode 139 may be formed over the thin film transistor with the insulating film 137 interposed therebetween as in the step illustrated in FIG. 6C.

This embodiment can be implemented in appropriate combination with any of the other embodiments.

(Embodiment 5)

Thin film transistors are manufactured, and a semiconductor device having a display function (also referred to as a display device) can be manufactured using the thin film transistors in a pixel portion and also in a driver circuit. Further, part or the whole of the driver circuit which includes thin film transistors can be formed over the same substrate as the pixel portion, whereby a system-on-panel can be formed.

The display device includes a display element. As the display element, a liquid crystal element (also referred to as a liquid crystal display element) or a light-emitting element (also referred to as a light-emitting display element) can be used. The light-emitting element includes, in its category, an element whose luminance is controlled by a current or a voltage, and specifically includes an inorganic EL (electroluminescence) element, an organic EL element, and the like. Furthermore, the display device may include a display medium whose contrast is changed by an electric effect, such as electronic ink.

In addition, the display device includes a panel in which the display element is sealed, and a module in which an IC or the like including a controller is mounted on the panel. Further, an embodiment of the present invention relates to one mode of an element substrate before the display element is completed in a process of manufacturing the display device, and the element substrate is provided with a plurality of pixels each having a means for supplying current to the display element. Specifically, the element substrate may be in a state where only a pixel electrode of the display element is formed, a state in which a conductive film to be a pixel electrode is formed but is not etched yet to form the pixel electrode, or any of the other states.

Note that a display device in this specification refers to an image display device, a display device, or a light source (including a lighting device). Further, the display device also includes any of the following modules in its category: a module to which a connector such as a flexible printed circuit (FPC), a tape automated bonding (TAB) tape, or a tape carrier package (TCP) is attached; a module having a TAB tape or TCP provided with a printed wiring board at the end thereof; and a module having an integrated circuit (IC) that is directly mounted on a display element by a chip on glass (COG) method.

(Embodiment 6)

In this embodiment, a photoelectric conversion device that is one embodiment of a semiconductor device will be described. In the photoelectric conversion device described in this embodiment, a microcrystalline semiconductor film, as described in Embodiment 1, whose crystallinity is increased by reduction of the space between mixed phase grains, is used as a semiconductor film. The microcrystalline semiconductor film whose crystallinity is increased by reduction of the space between mixed phase grains is applicable to a semiconductor film having a function of photoelectric conversion, a semiconductor film having a conductivity type, or the like, and is preferably, in particular, applied to the semiconductor film having a function of photoelectric conversion. Further, the microcrystalline semiconductor film having high crystallinity and high uniformity of grain sizes of mixed phase grains can be provided at an interface between the semiconductor film having a function of photoelectric conversion or the semiconductor film having a conductivity type and another film. Further, the microcrystalline semiconductor film whose crystallinity is increased by reduction of the space between mixed phase grains can be provided at an interface between the

semiconductor film having a function of photoelectric conversion or the semiconductor film having a conductivity type and another film.

By employing the structure described above, resistance (series resistance) caused by the semiconductor film having a function of photoelectric conversion or the semiconductor film having a conductivity type can be reduced, resulting in improvement of characteristics. Further, it is possible to reduce optical and electrical loss at the interface between the semiconductor film having a function of photoelectric conversion or the semiconductor film having a conductivity type and another film, which can improve the photoelectric conversion efficiency. With reference to FIGS. 10A to 10E, one embodiment of a method for manufacturing a photoelectric conversion device will be described.

As illustrated in FIG. 10A, a first electrode 202 is formed over a substrate 200.

As the substrate 200, any of the substrates that can be used for the substrate 51 described in Embodiment 1 can be used as appropriate. Alternatively, a plastic substrate can be used. As the plastic substrate, it is preferable to use a substrate containing a thermosetting resin such as an epoxy resin, an unsaturated polyester resin, a polyimide resin, a bismaleimide-triazine resin, or a cyanate resin, or a substrate containing a thermoplastic resin such as a polyphenylene oxide resin, a polyetherimide resin, or a fluorine resin.

Note that the substrate 200 may have a texture structure. Accordingly, photoelectric conversion efficiency can be improved.

In this embodiment, light is incident on the back side (the lower side in the drawing) of the substrate 200; thus, a light-transmitting substrate is used. Note that when a structure is employed in which light is incident on a side of a second electrode 210 to be formed later (the upper side in the drawing), the substrate is not limited to a light-transmitting substrate. In this case, a semiconductor substrate containing a material such as silicon or a conductive substrate containing a metal material or the like may be used.

The first electrode 202 can be formed using a light-transmitting conductive material that can be used for the back gate electrode 139 described in Embodiment 2. The first electrode 202 is formed by a sputtering method, a CVD method, a vacuum evaporation method, a coating method, a printing method, or the like.

The first electrode 202 is formed to a thickness of 10 nm to 500 nm, preferably 50 nm to 100 nm. The sheet resistance of the first electrode 202 is set to about 20 Ω /sq. to 200 Ω /sq.

Note that in this embodiment, light is incident on the back side (the lower side in the drawing) of the substrate 200; thus, the first electrode 202 is formed using a light-transmitting conductive material. Note that when a structure is employed in which light is incident on a side of a second electrode 210 to be formed later (the upper side in the drawing), the material of the substrate is not limited to a light-transmitting conductive material. In such a case, the first electrode 202 can be formed using a conductive material that does not have a light-transmitting property such as aluminum, platinum, gold, silver, copper, titanium, tantalum, or tungsten. In particular, when a material that easily reflects light, such as aluminum, silver, titanium, or tantalum, is used, photoelectric conversion efficiency can be sufficiently improved.

Like the substrate 200, the first electrode 202 may have a texture structure. Further, an auxiliary electrode formed using a low-resistance conductive material may be separately formed so as to be in contact with the first electrode 202.

Next, as illustrated in FIG. 10B, a semiconductor film 204 having the first conductivity type is formed over the first

electrode 202. The semiconductor film 204 having the first conductivity type is typically formed using a semiconductor film containing a semiconductor material to which an impurity element imparting a conductivity type is added. Silicon is suitable as a semiconductor material, in terms of productivity, price, and the like. When silicon is used as the semiconductor material, phosphorus or arsenic, which imparts n-type conductivity, or boron or aluminum, which imparts p-type conductivity, or the like is used as the impurity element imparting a conductivity type.

In this embodiment, light is incident on the back side (the lower side in the drawing) of the substrate 200; thus, the conductivity type (the first conductivity type) of the semiconductor film 204 having the first conductivity type is preferably p-type. This is because, for instance, the diffusion length of holes is short owing to the lifetime of a hole which is as short as about half the lifetime of an electron, and because more electrons and holes are formed on the side where light is incident on a semiconductor film 206 having a function of photoelectric conversion. When the first conductivity type is p-type, current can be extracted before holes are annihilated, whereby a decrease in photoelectric conversion efficiency can be suppressed. Note that when the above problems do not occur, for example, when the semiconductor film 206 having a function of photoelectric conversion is sufficiently thin, the first conductivity type may be n-type.

There are other semiconductor materials which can be used for the semiconductor film 204 having the first conductivity type; for example, silicon carbide, germanium, gallium arsenide, indium phosphide, zinc selenide, gallium nitride, and silicon germanium are given. Further, a semiconductor material containing an organic material, a semiconductor material containing a metal oxide, or the like can be used. The material can be selected as appropriate in consideration of the semiconductor film 206 having a function of photoelectric conversion.

Although there is no particular limitation on the crystallinity of the semiconductor film 204 having the first conductivity type, it is preferable to use the microcrystalline semiconductor film whose crystallinity is increased by reduction of the space between mixed phase grains, which is described in Embodiment 1, as the semiconductor film 204 having the first conductivity type. This is because in this case, as compared with the case of using a conventional microcrystalline semiconductor film, it is possible to reduce series resistance and to suppress optical and electrical loss at the interface between the microcrystalline semiconductor film whose crystallinity is increased and another film. It is needless to say that another semiconductor such as an amorphous semiconductor, a polycrystalline semiconductor, and a single crystal semiconductor can also be used.

Like the substrate 200, the semiconductor film 204 having the first conductivity type may have a texture structure.

The semiconductor film 204 having the first conductivity type can be formed by a plasma CVD method using diborane and a deposition gas containing silicon. Further, the semiconductor film 204 having the first conductivity type is formed to a thickness of 1 nm to 100 nm, preferably 5 nm to 50 nm.

Alternatively, the semiconductor film 204 having the first conductivity type may be formed as follows: a silicon film to which an impurity element imparting a conductivity type is not added is formed by a plasma CVD method or the like; and boron is added by an ion implantation method or the like.

Next, as illustrated in FIG. 10C, the semiconductor film 206 having a function of photoelectric conversion is formed over the semiconductor film 204 having the first conductivity type. For the semiconductor film 206 having a function of

31

photoelectric conversion, a semiconductor film formed using a semiconductor material which is similar to that of the semiconductor film **204** is used. In other words, as the semiconductor material, silicon, silicon carbide, germanium, gallium arsenide, indium phosphide, zinc selenide, gallium nitride, silicon germanium, or the like is used. In particular, silicon is preferably used. Alternatively, a semiconductor material containing an organic material, a semiconductor material containing a metal oxide, or the like can be used.

As the semiconductor film **206** having a function of photoelectric conversion, the microcrystalline semiconductor film whose crystallinity is increased by reduction of the space between mixed phase grains, such as that described in Embodiment 1, is preferably used. By applying the microcrystalline semiconductor film whose crystallinity is increased by reduction of the space between mixed phase grains, such as that described in Embodiment 1, to the semiconductor film, it is possible to reduce series resistance and to suppress optical and electrical loss at the interface between the microcrystalline semiconductor film whose crystallinity is increased and another film as compared with the case of using a conventional microcrystalline semiconductor film.

The semiconductor film **206** having a function of photoelectric conversion needs to absorb light sufficiently, and thus preferably has a thickness of about 100 nm to 10 μ m.

Next, as illustrated in FIG. **10D**, a semiconductor film **208** having the second conductivity type is formed over the semiconductor film **206** having a function of photoelectric conversion. In this embodiment, the second conductivity type is n-type. The semiconductor film **208** having the second conductivity type can be formed using a material such as silicon to which phosphorus is added as an impurity element imparting a conductivity type. Semiconductor materials that can be used for the semiconductor film **208** having the second conductivity type are similar to those for the semiconductor film **204** having the first conductivity type.

The semiconductor film **208** having the second conductivity type can be formed in a manner similar to that of the semiconductor film **204** having the first conductivity type. For example, the semiconductor film **208** having the second conductivity type can be formed by a plasma CVD method using phosphine and a deposition gas containing silicon. As the semiconductor film **208** having the second conductivity type, the microcrystalline semiconductor film whose crystallinity is increased by reduction of the space between mixed phase grains, which is described in Embodiment 1, is preferably used.

In this embodiment, light is incident on the back side (the lower side in the drawing) of the substrate **200**; thus, the conductivity type of the semiconductor film **208** having the second conductivity type is n-type; however, one embodiment of the disclosed invention is not limited thereto. When the semiconductor film **204** having the first conductivity type is n-type, the semiconductor film **208** having the second conductivity type is p-type.

Then, as illustrated in FIG. **10E**, the Second electrode **210** is formed over the semiconductor film **208** having the second conductivity type. The second electrode **210** is formed using a conductive material such as metal. They can be formed using a material that easily reflects light, such as aluminum, silver, titanium, or tantalum. Such a material is preferably used because light that fails to be absorbed by the semiconductor film **206** can be incident on the semiconductor film **206** again; thus, photoelectric conversion efficiency can be improved.

As a method of forming the second electrode **210**, there are a sputtering method, a vacuum evaporation method, a CVD

32

method, a coating method, a printing method, and the like. Further, the second electrode **210** is formed to a thickness of 10 nm to 500 nm, preferably 50 nm to 100 nm.

Note that in this embodiment, light is incident on the back side (the lower side in the drawing) of the substrate **200** and the second electrode **210** is formed using a conductive material which does not have a light-transmitting property, but the structure of the second electrode **210** is not limited thereto. For example, when light is incident on the second electrode **210** side (the upper side in the drawing), the second electrode **210** can be formed using any of the light-transmitting conductive materials for the first electrode **202**.

Further, an auxiliary electrode formed using a low-resistance conductive material may be formed so as to be in contact with the second electrode **210**.

By the above method, it is possible to manufacture a photoelectric conversion device in which a microcrystalline semiconductor film whose crystallinity is increased by reduction of the space between the mixed phase grains is used as any of a semiconductor film having a function of photoelectric conversion, a semiconductor film having the first conductivity type, and a semiconductor film having the second conductivity type. This can enhance the photoelectric conversion efficiency of a photoelectric conversion device. Note that, as long as the microcrystalline semiconductor film whose crystallinity is increased by reduction of the space between the mixed phase grains is used as one of the semiconductor film having a function of photoelectric conversion, the semiconductor film having the first conductivity type, and the semiconductor film having the second conductivity type, the film to which the microcrystalline semiconductor film is applied can be changed as appropriate. Further, when the microcrystalline semiconductor films whose crystallinity is increased by reduction of the space between the mixed phase grains are used as more than one of the above semiconductor films, the photoelectric conversion efficiency can be more effectively improved.

Note that although a photoelectric conversion device having one unit cell is described in this embodiment, a photoelectric conversion device in which two or more unit cells are stacked as appropriate may be provided.

This embodiment can be implemented in appropriate combination with any of the other embodiments. (Embodiment 7)

A semiconductor device disclosed in this specification can be applied to a variety of electronic devices (including game machines). Examples of the electronic devices include television sets (also referred to as televisions or television receivers), monitors of computers or the like, cameras such as digital cameras or digital video cameras, digital photo frames, cellular phones (also referred to as mobile phones or cellular phone sets), portable game consoles, portable information terminals, audio reproducing devices, large-sized game machines such as pachinko machines, electronic paper, and the like. The electronic paper can be used for electronic devices for displaying information in a variety of fields. For example, an electronic paper can be applied to electronic book readers (e-book readers), posters, digital signage, public information displays (PIDs), advertisements in vehicles such as trains, and displays of various cards such as credit cards. FIG. **11** illustrates an example of the electronic devices.

FIG. **11** illustrates an example of an electronic book reader. For example, an electronic book reader **2700** includes two housings, a housing **2701** and a housing **2703**. The housing **2701** and the housing **2703** are combined with the use of a hinge **2711** so that the electronic book reader **2700** can be

33

opened and closed using the hinge 2711 as an axis. With such a structure, the electronic book reader 2700 can be handled like a paper book.

A display portion 2705 and a photoelectric conversion device 2706 are incorporated in the housing 2701. A display portion 2707 and a photoelectric conversion device 2708 are incorporated in the housing 2703. The display portion 2705 and the display portion 2707 may display a continuous image or different images. In the case where the display portions display different images, for example, a display portion on the right (the display portion 2705 in FIG. 11) can display text and a display portion on the left (the display portion 2707 in FIG. 11) can display graphics.

FIG. 11 illustrates an example in which the housing 2701 is provided with an operation portion and the like. For example, the housing 2701 is provided with a power switch 2721, operation keys 2723, a speaker 2725, and the like. Pages can be turned with the operation keys 2723. Note that a keyboard, a pointing device, and the like may be provided on the same surface as the display portion of the housing. Moreover, an external connection terminal (an earphone terminal, a USB terminal, a terminal connectable to an AC adapter or a variety of cables such as a USB cable, or the like), a storage medium insertion portion, and the like may be provided on the back surface or the side surface of the housing. Moreover, the electronic book reader 2700 may have a function of an electronic dictionary.

The electronic book reader 2700 may be configured to wirelessly transmit and receive data. Through wireless communication, desired book data or the like can be purchased and downloaded From an electronic book server.

EXAMPLE 1

In this example, a microcrystalline semiconductor film having high crystallinity, in which a space between mixed phase grains in a seed crystal is filled, can be formed by forming a microcrystalline semiconductor film in three steps: formation of a seed crystal under a first condition, formation of a first microcrystalline semiconductor film under a second condition, and formation of a second microcrystalline semiconductor film under a third condition as described in Embodiment 1.

First, a method for forming a microcrystalline semiconductor film using the method described in Embodiment 1 will be described.

A silicon nitride film with a thickness of 300 nm was formed as an insulating film over a glass substrate (EAGLE XG manufactured by Corning Incorporated), and the silicon nitride film was exposed to plasma generated using a mixed gas of hydrogen and oxygen. Then, a seed crystal with a thickness of 5 nm was formed by a plasma CVD method over the silicon nitride film, a first microcrystalline film with a thickness of 25 nm was formed by a plasma CVD method over the silicon nitride film and the seed crystal, and then a second microcrystalline semiconductor film with a thickness of 40 nm was formed by a plasma CVD method over the first microcrystalline semiconductor film.

The silicon nitride film was formed by plasma discharge performed under the following conditions: silane, hydrogen, nitrogen, and ammonia were introduced as source gas at flow rates of 15 sccm, 200 sccm, 180 sccm, and 500 sccm, respectively; the pressure in a process chamber was 100 Pa; the RF power supply frequency was 13.56 MHz; and the power of the RF power supply was 200 W. Note that in the deposition of the silicon nitride film, a parallel-plate plasma CVD apparatus was used, the temperature of an upper electrode was 250° C.,

34

the temperature of a lower electrode was 290° C., and the distance (the gap) between the upper electrode and the lower electrode was 30 mm.

The plasma treatment on the silicon nitride film was performed by plasma discharge for three minutes under the following conditions: hydrogen and oxygen were introduced into a process chamber at flow rates of 800 sccm and 200 sccm respectively, the pressure in the process chamber was 1250 Pa, and the power was 900 W. Note that for the plasma treatment, a parallel-plate plasma treatment apparatus was used, the temperature of an upper electrode was 250° C., the temperature of a lower electrode was 290° C., and the distance between the upper electrode and the lower electrode was 15 mm.

The seed crystal was formed by plasma discharge performed under the following conditions: silane, hydrogen, and argon were introduced as source gas at flow rates of 3 sccm, 750 sccm, and 750 sccm, respectively; the pressure in a process chamber was 1250 Pa; the RF power supply frequency was 13.56 MHz; and the power of the RF power supply was 90 W. Note that in the deposition of the seed crystal, a parallel-plate plasma CVD apparatus was used, the temperature of an upper electrode was 250° C., the temperature of a lower electrode was 290° C., and the distance between the upper electrode and the lower electrode was 15 mm.

The first microcrystalline semiconductor film was formed by plasma discharge performed under the following conditions: silane, hydrogen, and argon were introduced as source gas at flow rates of 2 sccm, 1500 sccm, and 1500 sccm, respectively; the pressure in a process chamber was 10000 Pa; the RF power supply frequency was 13.56 MHz; and the power of the RF power supply was 350 W. Note that in the deposition of the first microcrystalline semiconductor film, a parallel-plate plasma CVD apparatus was used, the temperature of an upper electrode was 250° C., the temperature of a lower electrode was 290° C., and the distance between the upper electrode and the lower electrode was 7 mm.

The deposition conditions other than the flow rate of silane for the second microcrystalline semiconductor film are similar to those for the first microcrystalline semiconductor film. A first period in which silane flows at a flow rate of 1 sccm for 10 seconds and a second period in which silane flows at a flow rate of 0.1 sccm were repeated. The time for which silane flows at a flow rate of 1 sccm is referred to as "High time", and the time for which silane flows at a now rate of 0.1 sccm is referred to as "Low time".

Second microcrystalline semiconductor films were deposited under the conditions where the time for which silane flows at a flow rate of 0.1 sccm (Low time) is 5 seconds, 10 seconds, 15 seconds, 20 seconds, 25 seconds, 30 seconds, 45 seconds, and 60 seconds. Then, the crystallinity of the microcrystalline semiconductor films was analyzed by Raman spectroscopy. In the graph of FIG. 12A, rhombuses represent the crystalline/amorphous peak intensity ratio (Ic/Ia) at three points in the respective microcrystalline semiconductor films, and rectangles represent the full width at half maximum (FWHM) of the peak at 520 cm⁻¹ in respective Raman spectra. In FIG. 12A, the left y-axis shows the Ic/Ia against Low time on the horizontal axis, and the right y-axis shows the FWHM against Low time on the horizontal axis.

As Low time becomes longer with respect to High time, the value of Ic/Ia becomes larger and the value of FWHM becomes smaller. This shows that when the time for which silane flows at a low flow rate (Low time) becomes longer with respect to the time for which silane flows at a high flow rate (High time), the crystallinity of the microcrystalline semiconductor film is increased.

Next, microcrystalline semiconductor films were formed by setting High time at 10 seconds and Low time at 15 seconds, 30 seconds, and 60 seconds in the deposition of the second microcrystalline semiconductor film, and a microcrystalline semiconductor film was formed as a comparative example by setting High time at 10 seconds and Low time at 5 seconds. Then, the size of a crystallite in a mixed phase grain in the above microcrystalline semiconductor films was evaluated by in-plane X-ray diffraction (in-plane XRD). The film density of the respective microcrystalline semiconductor films was analyzed by X-ray reflectometry (XRR). The results are shown in FIG. 12B. In FIG. 12B, the left y-axis shows the size of a crystallite against Low time on the horizontal axis. Bars individually indicate the size of crystallites having (111) orientation, (220) orientation, and (311) orientation. Further, in the bar chart, the bar with vertical hatching indicates the size of a crystallite having (111) orientation, the bar with hatching that is oblique to the upper right indicates the size of a crystallite having (220) orientation, and the bar with hatching that is oblique to the upper left indicates the size of a crystallite having (311) orientation.

The right y-axis and rhombuses show the film density against Low time on the horizontal axis. Note that in the XRR analysis, fitting was performed on four-layer structure models: an interface layer with a base film, a main layer, a surface roughness layer (1), and a surface roughness layer (2), into which the microcrystalline semiconductor film was divided from the silicon nitride film side. The average density of the four layers is largely affected by the surface roughness layer (1) and the surface roughness layer (2). Thus, in order to separately evaluate only an increase and decrease of a space between mixed phase grains in the microcrystalline semiconductor films, the value of the main layer was compared.

In FIG. 12B, the film density of the microcrystalline semiconductor films in which the second microcrystalline semiconductor film is deposited under a condition where Low time is 5 seconds or more is 2.30 g/cm^3 or higher. Since the film density of single crystal silicon is 2.33 g/cm^3 , it can be said that there is extremely little space between mixed phase grains in any of the microcrystalline semiconductor films. Further, the Microcrystalline semiconductor films in which the second microcrystalline semiconductor film is deposited under a condition where Low time is longer than High time, include a crystallite having a size of 13 nm or more.

Next, SEM photographs of a microcrystalline semiconductor film formed under a condition where Low time is 60 seconds (referred to as Sample 1) and a microcrystalline semiconductor film formed under a condition where Low time is 5 seconds (referred to as Sample 2), which were observed with a scanning electron microscope, are shown in FIGS. 13A and 13B and FIGS. 14A and 14B. FIG. 13A and FIG. 14A are photographs of planes (magnified 0.2 million times), and FIG. 13B and FIG. 14B are photographs of cross sections (magnified 0.2 million times).

In the microcrystalline semiconductor film in FIG. 13A, more angular mixed phase grains than those in FIG. 14A are observed. In addition, a region projecting from the film surface can be seen prominently in the microcrystalline semiconductor film in FIG. 13B, as compared to the microcrystalline semiconductor film in FIG. 14B.

Next, TEM photographs of the formed microcrystalline semiconductor films of Sample 1 and Sample 2, which were observed with a high resolution transmission electron microscope, are shown in FIGS. 15A and 15B and FIGS. 16A and 16B. FIGS. 15A and 15B and FIGS. 16A and 16B are photographs of cross sections of the respective samples; FIG. 15A and FIG. 16A are photographs with a magnification of

0.5 million times and FIG. 15B and FIG. 16B are photographs with a magnification of 2 million times.

Mixed phase grains partly projecting from the surface are included more in the microcrystalline semiconductor film in FIG. 15A than in the microcrystalline semiconductor film in FIG. 16A. As shown in FIG. 15B, the projecting mixed phase grains have substantially the same contrast and have an orientation plane on the surface. Further, lines can be seen in the mixed phase grain, which shows that a twin crystal or a stacking fault is included therein.

Accordingly, by using the formation method described in Embodiment 1, a microcrystalline semiconductor film which has high crystallinity and in which mixed phase grains are densely packed with extremely little space between adjacent mixed phase grains can be formed.

Comparative Example

Here, in the formation method of the second microcrystalline semiconductor film described in Example 1, the flow rates of silane and hydrogen were set constant without employing cycle flow; thus, a microcrystalline semiconductor film was formed. This microcrystalline semiconductor film will be described with reference to FIG. 17.

A silicon nitride film with a thickness of 300 nm was formed as an insulating film over a glass substrate (EAGLE XG manufactured by Corning Incorporated), and the silicon nitride film was exposed to plasma generated in a dinitrogen monoxide atmosphere. Then, a seed crystal with a thickness of 5 nm was formed by a plasma CVD method over the silicon nitride film, a first microcrystalline semiconductor film with a thickness of 25 nm was formed by a plasma CVD method over the silicon nitride film and the seed crystal, and then a second microcrystalline semiconductor film was formed by a plasma CVD method over the first microcrystalline semiconductor film.

The silicon nitride film was formed at a flow rate of the source gas and a power of the plasma CVD apparatus which were similar to those in Example 1. Note that in the parallel-plate plasma CVD apparatus, the temperature of the upper electrode was 200°C ., the temperature of the lower electrode was 300°C ., and the distance between the upper electrode and the lower electrode was 26 mm.

The plasma treatment on the silicon nitride film was performed by plasma discharge for three minutes under the following conditions: dinitrogen monoxide was introduced into a process chamber at a flow rate of 400 sccm, the pressure in the process chamber was 60 Pa, and the power was 900 W. Note that for the plasma treatment, a parallel-plate plasma treatment apparatus was used, the temperature of an upper electrode was 200°C ., the temperature of a lower electrode was 300°C ., and the distance between the upper electrode and the lower electrode was 30 mm.

In the deposition conditions of the seed crystal, the same flow rate of the source gas as Example 1 was employed. The power of the RF power supply was set to 150 W. in addition, in the parallel-plate plasma CVD apparatus, the temperature of the upper electrode was not controlled by a heater, the temperature of the lower electrode was set to 300°C ., and the distance between the upper electrode and the lower electrode was set to 7 mm.

The first microcrystalline semiconductor film was formed by plasma discharge performed under the following conditions: silane and hydrogen were introduced as source gas at flow rates of 2 scan and 3000 sccm respectively; the pressure in a process chamber was 10000 Pa; the RF power supply frequency was 13.56 MHz; and the power of the RF power

supply was 700 W. Note that in the deposition of the first microcrystalline semiconductor film, the parallel-plate plasma CVD apparatus was used, the temperature of the upper electrode was not controlled by a heater, the temperature of the lower electrode was 300° C., and the distance 5 between the upper electrode and the lower electrode was 7 mm.

In forming the second microcrystalline semiconductor film, the deposition conditions other than the flow rates of silane and hydrogen were similar to those for the first microcrystalline semiconductor film. Here, plasma discharge was performed for 2400 seconds at a flow rate of silane of 0.1 sccm and a flow rate of hydrogen of 300 sccm.

A SEM photograph of the microcrystalline semiconductor film formed in the above-described process, which was observed with a scanning electron microscope, is shown in FIG. 17. FIG. 17 is the photograph of a plane (magnified 0.2 million times). As can be noticed from FIG. 17, a mixed phase grain having an orientation plane cannot be observed in the microcrystalline semiconductor film formed as the comparative example. Further, the average crystalline/amorphous peak intensity ratio (Ic/Ia) in three points in the microcrystalline semiconductor film was 10.8, and the average full width at half maximum (FWHM) of the peaks at 520 cm⁻¹ in Raman spectra was 11.8. From these results, it is found that the crystallinity of the microcrystalline semiconductor film is not improved if cycle flow is not performed in the step for forming the second microcrystalline semiconductor film. Moreover, the thickness of the microcrystalline semiconductor film formed as the comparative example was 30.8 nm, which means microcrystalline semiconductor was hardly deposited in the step for forming the second microcrystalline semiconductor film.

From the above, it can be found that a microcrystalline semiconductor film having high crystallinity can be formed by employing cycle flow in the step for forming the second microcrystalline semiconductor film.

This application is based on Japanese Patent Application serial no. 2011-012496 filed with Japan Patent Office on Jan. 25, 2011, the entire contents of which are hereby incorporated by reference.

What is claimed is:

1. A method for manufacturing a microcrystalline semiconductor film, comprising the steps of:

forming a seed crystal over an insulating film by a plasma CVD method under a first condition;

forming a first microcrystalline semiconductor film on the seed crystal by a plasma CVD method under a second condition; and

forming a second microcrystalline semiconductor film on the first microcrystalline semiconductor film by a plasma CVD method under a third condition,

wherein the first condition is a condition that a deposition gas containing silicon is diluted by setting a flow rate of hydrogen to more than or equal to 50 times and less than or equal to 1000 times that of the deposition gas, and a pressure in a process chamber is higher than or equal to 67 Pa and lower than or equal to 50000 Pa,

wherein the second condition is a condition that a deposition gas containing silicon is diluted by setting a flow rate of hydrogen to more than or equal to 100 times and less than or equal to 2000 times that of the deposition gas, and a pressure in the process chamber is higher than or equal to 1333 Pa and lower than or equal to 50000 Pa,

wherein the third condition is a condition that a pressure in the process chamber is higher than or equal to 1333 Pa and lower than or equal to 50000 Pa, and a first period in

which microcrystalline semiconductor is deposited and a second period which is longer than the first period and in which an amorphous semiconductor region formed in the first period is selectively etched are alternately performed, and

wherein the microcrystalline semiconductor film is formed by the seed crystal, the first microcrystalline semiconductor film, and the second microcrystalline semiconductor film.

2. The method for manufacturing a microcrystalline semiconductor film according to claim 1, wherein the seed crystal comprises a mixed phase grain including both an amorphous region and a crystalline region.

3. The method for manufacturing a microcrystalline semiconductor film according to claim 1, wherein a flow rate of hydrogen is fixed and a flow rate of the deposition gas containing silicon is increased and decreased in the third condition.

4. The method for manufacturing a microcrystalline semiconductor film according to claim 1,

wherein the microcrystalline semiconductor film comprises a crystal grain,

wherein the crystal grain has an orientation plane, and wherein the crystal grain comprises a crystallite having a size of 13 nm or more on a top surface of the microcrystalline semiconductor film.

5. The method for manufacturing a microcrystalline semiconductor film according to claim 4, wherein the crystal grain projects from the top surface of the microcrystalline semiconductor film.

6. The method for manufacturing a microcrystalline semiconductor film according to claim 1, wherein the microcrystalline semiconductor film has a film density of higher than or equal to 2.25 g/cm³ and lower than or equal to 2.35 g/cm³.

7. The method for manufacturing a microcrystalline semiconductor film according to claim 1, wherein a rare gas is contained in the deposition gas.

8. A method for manufacturing a semiconductor device by using the method for manufacturing a microcrystalline semiconductor film according to claim 1.

9. A method for manufacturing a semiconductor device, comprising the steps of:

forming a gate electrode over a substrate;

forming a gate insulating film over the gate electrode;

forming a seed crystal over the gate insulating film under a first condition;

forming a first microcrystalline semiconductor film on the seed crystal under a second condition;

forming a second microcrystalline semiconductor film on the first microcrystalline semiconductor film under a third condition;

forming a semiconductor film comprising a microcrystalline semiconductor region and an amorphous semiconductor region over the second microcrystalline semiconductor film;

forming a first impurity semiconductor film over the semiconductor film;

forming an island-shaped second impurity semiconductor film by etching part of the first impurity semiconductor film;

forming an island-shaped first semiconductor stacked body by etching part of the seed crystal, part of the first microcrystalline semiconductor film, part of the second microcrystalline semiconductor film, and part of the semiconductor film;

forming a wiring over the island-shaped second impurity semiconductor film; and

39

forming a pair of impurity semiconductor films by etching the island-shaped second impurity semiconductor film, wherein the first condition is a condition that a deposition gas containing silicon is diluted by setting a flow rate of hydrogen to more than or equal to 50 times and less than or equal to 1000 times that of the deposition gas, and a pressure in a process chamber is higher than or equal to 67 Pa and lower than or equal to 50000 Pa,

wherein the second condition is a condition that a deposition gas containing silicon is diluted by setting a flow rate of hydrogen to more than or equal to 100 times and less than or equal to 2000 times that of the deposition gas, and a pressure in the process chamber is higher than or equal to 1333 Pa and lower than or equal to 50000 Pa, and

wherein the third condition is a condition that a pressure in the process chamber is higher than or equal to 1333 Pa and lower than or equal to 50000 Pa, and a first period in which microcrystalline semiconductor is deposited and a second period which is longer than the first period and in which an amorphous semiconductor region formed in the first period is selectively etched are alternately performed.

10. The method for manufacturing a semiconductor device according to claim 9, further comprising the step of forming an insulating region on a side surface of the island-shaped first semiconductor stacked body by exposing the side surface of the island-shaped first semiconductor stacked body to plasma, after the step of forming the island-shaped first semiconductor stacked body and before the step of forming the wiring.

11. The method for manufacturing a semiconductor device according to claim 9, wherein the seed crystal comprises a mixed phase grain including both an amorphous region and a crystalline region.

12. The method for manufacturing a semiconductor device according to claim 9, wherein a flow rate of hydrogen is fixed and a flow rate of the deposition gas containing silicon is increased and decreased in the third condition.

13. The method for manufacturing a semiconductor device according to claim 9, wherein a rare gas is contained in the deposition gas.

40

14. The method for manufacturing a semiconductor device according to claim 9, further comprising the steps of:

forming a second semiconductor stacked body in which a microcrystalline semiconductor region and a pair of amorphous semiconductor regions are stacked, by etching part of the island-shaped first semiconductor stacked body;

forming an insulating film over the wiring, the pair of impurity semiconductor films, the second semiconductor stacked body, and the gate insulating film; and

forming a back gate electrode and a pixel electrode over the insulating film.

15. The method for manufacturing a semiconductor device according to claim 14, wherein the gate electrode and the back gate electrode are provided substantially parallel to each other.

16. The method for manufacturing a semiconductor device according to claim 14, wherein the gate electrode and the back gate electrode are electrically connected to each other.

17. The method for manufacturing a semiconductor device according to claim 14, wherein the back gate electrode is in a floating state.

18. The method for manufacturing a semiconductor device according to claim 14, wherein the back gate electrode and the pixel electrode are formed at a same time.

19. The method for manufacturing a semiconductor device according to claim 9,

wherein the second microcrystalline semiconductor film is formed to comprise a crystal grain,

wherein the crystal grain comprises a crystallite having a size of 13 nm or more on a top surface of the second microcrystalline semiconductor film.

20. The method for manufacturing a semiconductor device according to claim 19, wherein the crystal grain projects from the top surface of the second microcrystalline semiconductor film.

21. The method for manufacturing a semiconductor device according to claim 9, a microcrystalline semiconductor film formed by the seed crystal, the first microcrystalline semiconductor film, and the second microcrystalline semiconductor film has a film density of higher than or equal to 2.25 g/cm^3 and lower than or equal to 2.35 g/cm^3 .

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 9,048,327 B2
APPLICATION NO. : 13/355340
DATED : June 2, 2015
INVENTOR(S) : Tetsuhiro Tanaka et al.

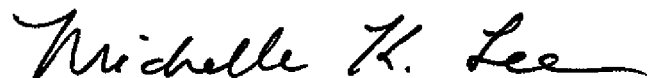
Page 1 of 3

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification:

Col. 1, line 27, "Film" should read --film--
Col. 2, line 34, "thereof" should read --thereof.--
Col. 3, line 43, "filth" should read --film--
Col. 4, line 8, "in a" should read --(i.e. in a--
Col. 4, line 29, "method," should read --method--
Col. 4, line 37, "which" should read --in which--
Col. 4, line 39, "second." should read --second--
Col. 5, line 26, "Film" should read --film--
Col. 5, line 31, "SEM." should read --SEM--
Col. 5, line 54, "film. 55" should --film 55--
Col. 6, line 11, "(1-IFS)" should read --(HFS)--
Col. 6, line 19, "percentages," should read --percentages--
Col. 7, line 16, "neon,." should read --neon.--
Col. 7, line 61, "he" should read --be--
Col. 8, line 55, "he" should read --be--
Col. 10, line 41, "be." should read --be--

Signed and Sealed this
First Day of December, 2015



Michelle K. Lee
Director of the United States Patent and Trademark Office

In the Specification:

Col. 10, line 65, “microcrystalline.” should read --microcrystalline--

Col. 11, line 12, “condition.” should read --condition--

Col. 11, line 25, “in” should read --In--

Col. 11, line 29, “Oak” should read --silane--

Col. 13, line 5, “h” should read --t₂--

Col. 13, lines 14 and 15, “however;” should read --however,--

Col. 13, line 45, “h” should read --b--

Col. 15, line 45, “he” should read --be--

Col. 16, line 31, “nun” should read --nm--

Col. 16, line 60, “513,” should read --5B,--

Col. 17, line 52, “thin” should read --film--

Col. 19, line 1, “oldie” should read --of the--

Col. 20, line 2, “oldie” should read --of the--

Col. 22, line 11, “ease” should read --case--

Col. 22, line 21, “he” should read --be--

Col. 22, line 24, “he” should read --be--

Col. 24, line 45, “embodiment;” should read --embodiment,--

Col. 25, line 24, “Alternatively;” should read --Alternatively,--

Col. 26, line 39, “semiconductor.” should read --semiconductor--

Col. 27, line 26, “Embodiment” should read --Embodiment 2;--

Col. 28, line 30, “he” should read --be--

Col. 31, line 15, “filth” should read --film--

Col. 31, line 56, “Second” should read --second--

Col. 33, line 31, “From” should read --from--

Col. 34, line 45, “now” should read --flow--

CERTIFICATE OF CORRECTION (continued)

Page 3 of 3

U.S. Pat. No. 9,048,327 B2

In the Specification:

Col. 35, line 41, "Microcrystalline" should read --microcrystalline--

Col. 35, line 64, "16A." should read --16A--

Col. 36, line 56, "in" should read --In--

Col. 36, line 65, "scan" should read --sccm--

Col. 37, line 29, "semiconductor." should read --semiconductor--